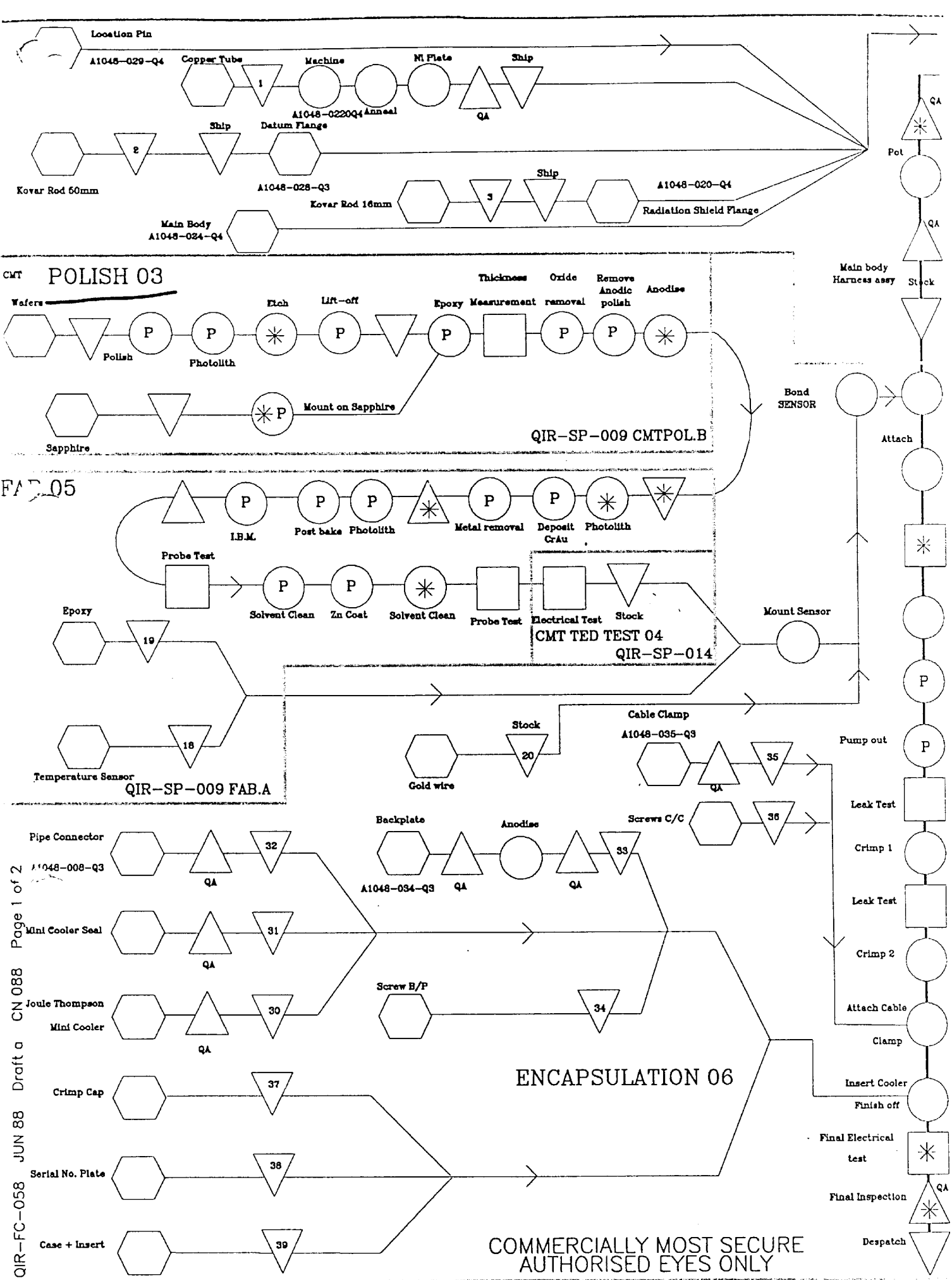
Location Pin
A1048-029-Q4
Copper Tube
1
Machine
A1048-0220Q4
Anneal
Ni Plate
QA
Ship
Ship
Datum Flange
2
Kovar Rod 50mm
A1048-028-Q3
Kovar Rod 16mm
3
Ship
A1048-020-Q4
Radiation Shield Flange
Main Body
A1048-024-Q4
QA
Pot
QA
Main body
Harness assy
Stock
CMT
POLISH 03
Wafers
Polish
Photolith
Etch
Lift-off
Epoxy
Thickness
Measurement
Oxide
removal
Remove
Anodic
polish
Anodise
Mount on Sapphire
Sapphire
QIR-SP-009 CMTPOL.B
Bond
SENSOR
Attach
FAB 05
I.B.M.
Post bake
Photolith
Metal removal
Deposit
CrAu
Photolith
Probe Test
Solvent Clean
Zn Coat
Solvent Clean
Probe Test
Electrical Test
Stock
CMT TED TEST 04
QIR-SP-014
Mount Sensor
Epoxy
19
Temperature Sensor
18
QIR-SP-009 FAB.A
Stock
20
Gold wire
Cable Clamp
A1048-035-Q3
QA
35
Pump out
Leak Test
Crimp 1
Leak Test
Crimp 2
Attach Cable
Clamp
Insert Cooler
Finish off
Final Electrical
test
Final Inspection
QA
Despatch
Backplate
A1048-034-Q3
QA
Anodise
QA
Screws C/C
36
33
Pipe Connector
A1048-008-Q3
QA
32
Mini Cooler Seal
QA
31
Joule Thompson
Mini Cooler
QA
30
Screw B/P
34
Crimp Cap
37
Serial No. Plate
38
Case + Insert
39
ENCAPSULATION 06
COMMERCIALLY MOST SECURE
AUTHORISED EYES ONLY
Page 1 of 2
CN 088
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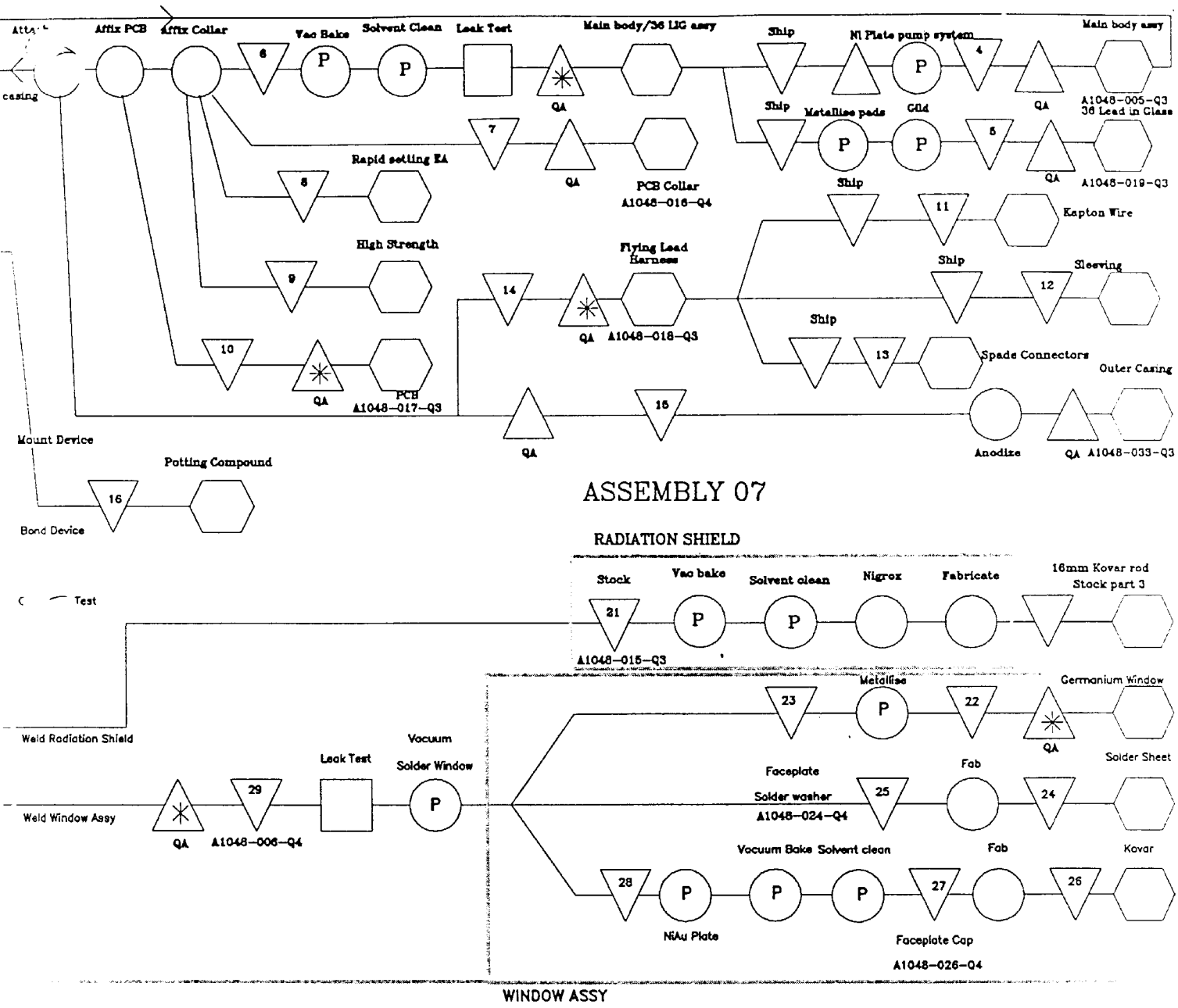


ASSEMBLY 07

WINDOW ASSY

SYMBOL	FUNCTION
⬡	Parts/Material Procurement
□	TEST
○	OPERATION
△	INSPECTION
▽	STOCK OR SHIPMENT
✳	DENOTES CRITICAL
P	DENOTES PROPRIETARY

INFRA-RED DETECTOR CONFIGURATION FLOW CHART

(HRC Dewar)

GEC Hirst Research Centre

JOULE-THOMSON MINICOOLERS

Principal of Operation

The Joule-Thompson minicooler is designed to be a close fit into the precision bore tube of the vacuum encapsulation (dewar) and to provide cryogenic cooling for the I.R. detector situated on the heat sink of the dewar.

The minicooler is basically a finned tube counter flow heat exchanger wound on a former tube.High pressure gas (max 40MPa)flows through the heat exchanger tube to the expansion nozzle where it expands isenthalpically to around atmospheric pressure.The expansion causes a reduction in the gas temperature,the cold low pressure gas is then constrained to flow back over the outside of the heat exchanger to be exhausted to atmosphere.

The action given above removes heat from the walls of the precision bore tube,thus cooling the detector,and also precools the incoming gas.The cumulative cooling effect rapidly reduces the temperature of the incoming gas to a point where the isenthalpic expansion causes a change of phase and a mixture of gas and liquid sprays out of the expansion nozzle.The liquid collected between the cooler and the dewar heat sink continually boils off removing conducted and radiant heat from the .I.R. detector.The change from the liquid to the gas phase occures at a constant temperature for a given vapour pressure over the liquid,for air this temperature is 79k at one atmosphere and for nitrogen it is 77k at one atmosphere.

The minicooler used by this department work on the above principal but with the addition of a gas reulation mechanism which senses the presence of the liquified gas and reduces the incoming gas flow,and thus the amount of liquid produced,to balance the conductive and radiant heat load of the detector.i(SEE FIGS 2 /3)

CLEANLINESS AND COMPATIBILITY OF GASES AND FITTINGS

Because of the small size of the orifice (0.1mm) and the regulation mechanism it is essential that contaminants do not reach the cooler.There are two main sources of contamination:-

1)Particles from a dirty pipe or valve and also from the gas supply if a point of use filter is not used.

2)Contaminated gas supply ie.containing water,hydrocarbons (oil) and carbon dioxide.

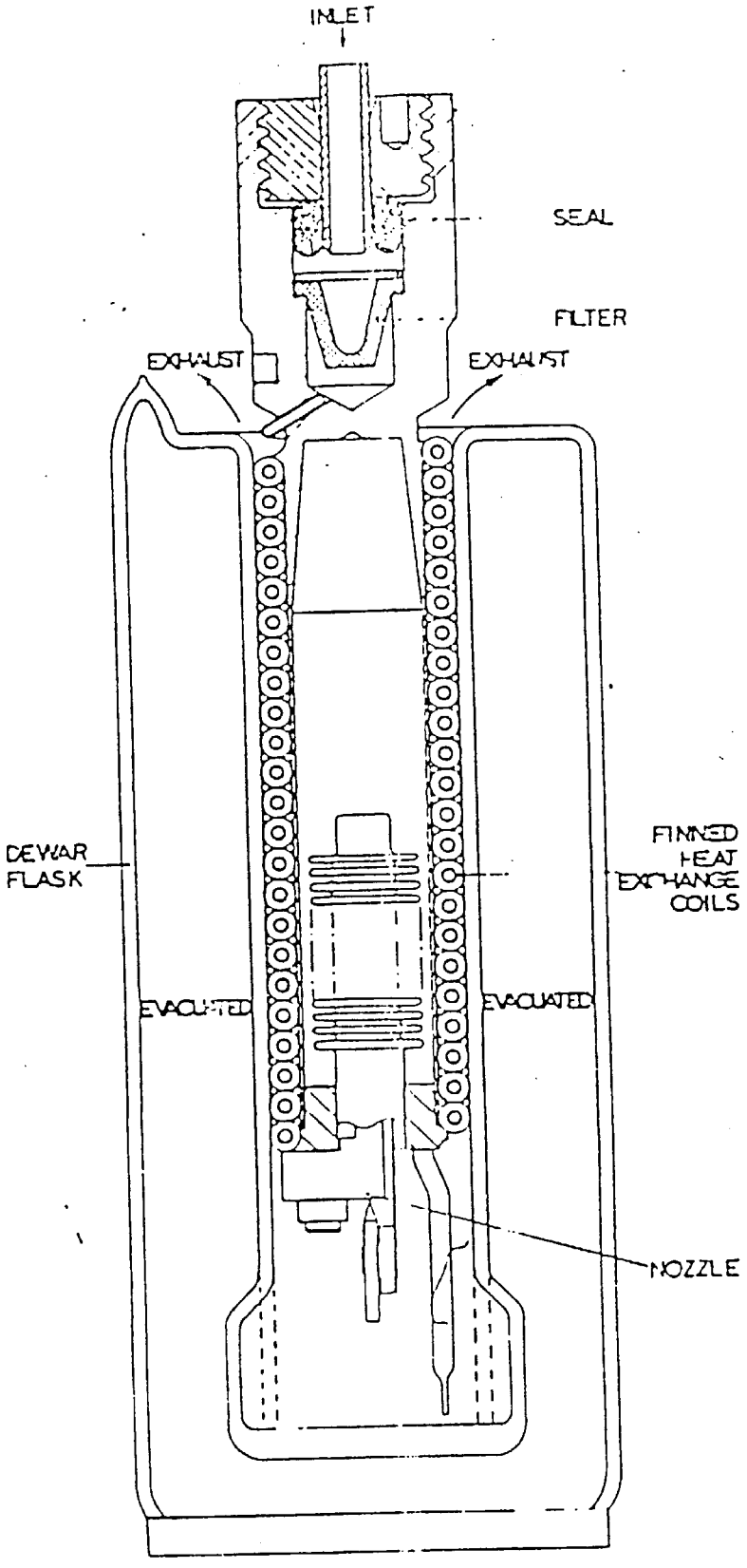

INLET
SEAL
FILTER
EXHAUST
EXHAUST
DEWAR FLASK
FINNED HEAT EXCHANGE COILS
EVACUATED
EVACUATED
NOZZLE

FIGURE 1

The gas must therefore be precleaned by the supplier,eg. white spot nitrogen,or by a gas cleaning plant when useing a compressor. The standard laid down for service requirements for minicoolers is given in AvP 32 chapter 410.All components and pipework associated with the use of minicoolers will arrive from the supplier cleaned to this standard and MUST be maintained at this standard if the coolers are to function reliably.

SYSTEM HANDLING

To preserve the integrity of a pure gas system it is essential that the following rules be observed:-

1)Observe the safety instructions for high pressure gas systems,a copy of which is available in the laboratory.

2)Ensure that servicing equipment,tools,operators hands and work area are clean.

3)The complete system is compatible to Pure Air standards.

4)On shutting down a system that a small pressure is trapped in the system to prevent contamination by back diffusion.

4)All disconnected components are efficiently blanked to prevent the ingress of contaminants.

5)Minicooler handling instructions are observed.

6)Do not contaminate a pure gas system by blowing through it by mouth or an ordinary compressed air line.ONLY USE PURE GAS.

7)The permitted gases are AIR,NITROGEN and ARGON.

8)Do not leave pipework exposed to atmosphere.

9)Always use a POINT OF USE FILTER.

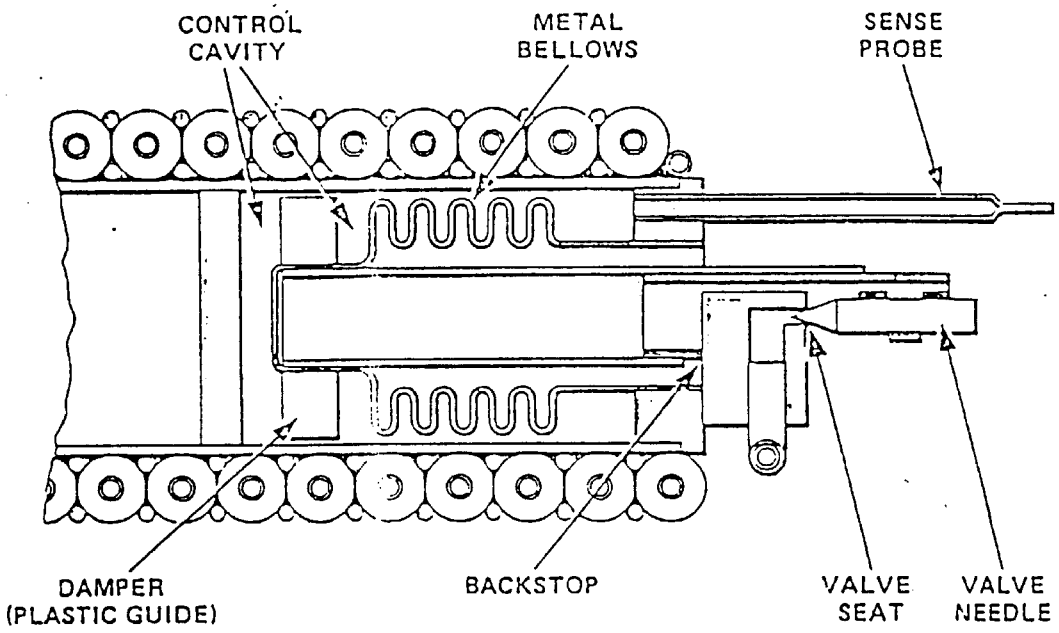
10)Always use WHITE SPOT gases if bottled gas is to be used.

COOLER HANDLING INSTRUCTIONS

1)The cooler should be handled as little as possible and then ONLY BY COOLER HEAD ie. the end conected to the pipework.

2)When not in use store in the transit tube in Silica Gel cabinet.

3)Do not touch the needle assembly or sense probe.



STANDARD SELF REGULATING MINICOOLER

FIGURE 2

4)When inserting or withdrawing a cooler from a dewar the cooler MUST be turned CLOCKWISE as veiwed along the axis of the cooler from the head end.

5)Do not remove the cooler from the dewar when cold.

6)Do not attempt to clean the needle assembly area.

A.R.POPLE 23-2-1984.

and in the cells of a battery during electrolysis". In this paper Joule concludes as a result of his experiments that "when a current of voltaic electricity is propagated along a metallic conductor, the heat evolved in a given time is proportional to the resistence of the conductor multiplied by the square of the electric intensity". In modern terminology the law would be stated thus: The heat evolved in a circuit in a given time when an electric current flows through it is proportional to the square of the current and the resistance of the circuit.

Since the heat evolved is proportional to the square of the current it is independent of current direction.

The law may be derived theoretically using Ohm's law. Consider a circuit through which a current of I amperes flows, the potential difference across the circuit being V volts. Then, by definition of V, the rate at which energy is dissipated in the circuit per second is $VI \times 10^7$ ergs. In a time t therefore the energy dissipated is $VIt \times 10^7$ ergs.

But, by Ohms law $V = IR$, where R is the resistance of the circuit.

$\therefore$ Energy dissipated $= I^2Rt \times 10^7$ ergs.

$\therefore$ Heat produced, $H = \dfrac{I^2Rt \times 10^7}{J}$ calories.

where J is the mechanical equivalent of heat $= 4{\cdot}18 \times 10^7$ ergs/calorie.

$\therefore H = \dfrac{I^2Rt}{4{\cdot}18}$

This can be regarded as the mathematical statement of Joule's law.

See also: Ohm's law.

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SMITH C.J. (1954) *Electricity and Magnetism*, London: Arnold.

R.C. GLASS

JOULE-THOMSON EFFECT. The Joule-Thomson effect is the change in temperature experienced by a stream of gas when its pressure decreases in a prescribed manner. The pressure drop takes place in a valve, capillary, porous plug or other throttling device. In the original experiment in 1862 Joule and Thomson used a porous plug. No heat is allowed to enter or leave the stream of gas. The rate of flow should be so low that turbulence and sound waves are not set up, nor is there an appreciable gain of kinetic energy. Under these conditions the net work done by unit mass of the gas is $(p_2v_2 - p_1v_1)$. That is,

$$\Delta w = p_2v_2 - p_1v_1.$$

If the internal energy of unit mass is u_1 before and u_2 after throttling,

$$\Delta u = u_2 - u_1.$$

Since there was not heat transfer, the first law of thermodynamics give us

$$u_2 - u_1 + p_2v_2 - p_1v_1 = 0$$

or

$$u_2 + p_2v_2 = u_1 + p_1v_1$$

or

$$h_2 = h_1$$

where h is the specific enthalpy.

The Joule-Thomson process, is therefore, an isenthalpic expansion.

The **integral Joule-Thomson effect** is the total change in temperature caused by a finite drop in pressure. When multiplied by the specific heat C_p at the final pressure, it is a measure of the possible cooling or heating effect of a throttling process between the two pressure levels. The **differential Joule-Thomson effect** can be expressed in terms of the specific heat and the equation of state of the gas as follows:

$$\left(\frac{\partial T}{\partial p}\right)_h = \frac{T\left(\frac{\partial v}{\partial T}\right)_p - v}{b_p}$$

For a given gas the differential Joule-Thomson effect, $(\partial T/\partial p)_h$, varies with both temperature and pressure and is negative at relatively high temperatures at all pressures. At lower temperatures it is positive in the low pressure range and becomes negative at high pressures. The temperature at which the differential Joule-Thomson effect become zero for a given pressure is said to be the **inversion temperature.** Gases vary widely as to their inversion temperatures.

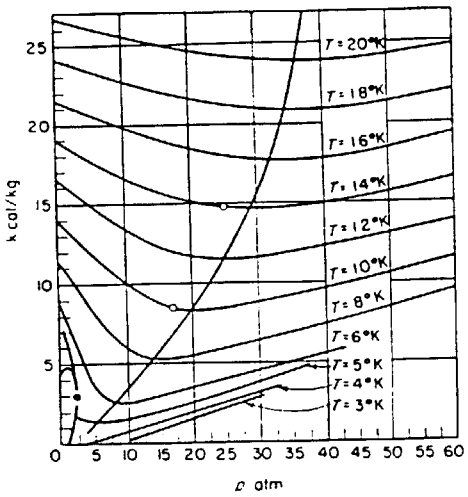
An enthalpy-temperature diagram such as the one for helium by Zelmanov shown in Fig. 1 is useful for demonstrating the variation of the Joule-Thomson effect with temperature and pressure. Starting with the gas at a chosen temperature and pressure and moving horizontally (constant enthalpy) to the left note the change in temperature. If the expansion begins at a point to the right of the diagonal curve, the temperature rises with falling pressure until the curve is crossed. Thereafter the temperature falls. This diagonal line drawn through the lowest point of the isothermals is the locus of inversion temperatures for helium. For the maximum cooling effect by Joule-Thomson expansion beginning at 14°K, for instance, the starting pressure should not exceed 30atm. If the initial temperature is 10°K, then the initial pressure should not exceed 20atm.

The Joule-Thomson effect has been extensively used in the liquefaction of gases. For this purpose it is obvious that the gas must be below its inversion temperature. Hydrogen and helium whose inversion temperatures lie far below room temperature must be suitably pre-cooled. The enthalpy of the compressed gas must be lower than that of the expanded gas at the same temperature. This deficit of enthalpy is an exact measure of the possible refrigerative effect upon expansion.

In order to take advantage of the relatively small refrigerative effect a counterflow heat exchanger is used between the precooler and the expansion valve. The heat exchanger consists of two lengthy conduits

Encyclopaedic Dictionary of Physics
Pergamon 1961

in good thermal contact with each other. The slightly cooler expanded gas from the valve absorbs heat from the incoming compressed stream causing the latter to arrive at the valve at a progressively lower temperature until the condensing point of the gas is finally reached.



Variation of enthalpy with pressure at several temperatures.

The fraction of the gas liquefied is a function of the difference in specific enthalpy at the pre-cooler temperature between high and low pressure, the latent heat of the liquid and the efficiency of the heat exchanger. The fraction actually liquefied, ε, is given by the equation

$$\varepsilon = \frac{h_2 - h_1}{h_2 - h_3}.$$

The specific enthalpy of the compressed gas entering the heat exchanger is designated by h_1, that of the expanded gas leaving by h_2 and the enthalpy of the liquid phase by h_3.

S.C. COLLINS

JOULE-THOMSON VALVE. A throttling device for the isenthalpic expansion of the working fluid in refrigerators using the Joule–Thomson effect. A common form of valve has a circular orifice partially closed by a fine adjustable needle.

See also: Joule–Thomson effect.

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COLLINS S.C. and CANNADAY R.L. (1958) *Expansion Machines for Low-Temperature Processes*, Oxford: The University Press.

DAUNT J.G. *Handbuch der Physik—Low Temperature Physics* Vol. 1, Berlin: Springer.

J.A. HULBERT

JOULE (UNIT). The absolute Joule is defined as a unit of mechanical energy, equal to 10^7 ergs.

The international Joule is defined as the work done per second in a resistance carrying a current of one international ampere, the potential difference across the resistance being one international ohm.

One International Joule = 1·00019 absolute Joules.

See also: Mechanical equivalent of heat. Various articles beginning "Units".

JOVIGNOT TEST. The Jovignot test is used to determine the ductility of metal sheet. The circular plate to be tested is clamped at the edges and subjected to fluid pressure on one side. The sheet deforms into a segment of a sphere and eventually ruptures. The cupping coefficient is equivalent to the average increase in surface area when fracture occurs per unit area of sheet that is free to bulge.

S.F. PUGH

JULIAN DATE. For scientific and chronological purposes, the expression of dates by reference to year, month and day is a clumsy expedient, and the interval between two dates involves unnecessarily awkward calculations. The Renaissance scholar Joseph Justus Scaliger suggested in 1582 a system of reckoning by successive days, independently of various calendars and chronological epochs, by which all dates were to be referred to an arbitrary "zero" date, January 1, 4713 B.C., which he chose in connexion with his work on early chronology. The date thus reckoned is known as the Julian date, so named by its founder in honour of his father, Julius Scaliger, and having absolutely no connexion with the Julian Calendar. Julian days are used to express the times of most astronomical observations; they are reckoned from noon, and parts of a day are expressed in decimals to the necessary degree of precision. On January 1, 1960, the Julian date was 2,435,934.

JUMP FREQUENCY OF ATOMS. The quantity K, appearing in the formula for the diffusion coefficient D for atoms in a solid, derived by considering the solid as consisting of layers of atoms:

$$D = K\delta^2 \qquad (1)$$

where δ is the distance between layers. $K\,\mathrm{d}t$ is the probability that a given atom in a layer A shall move into the adjacent layer B during the time $\mathrm{d}t$. K is a frequency analogous to the velocity constant of a unimolecular chemical reaction; the velocity for such reactions is approximately given by the semi-empirical formula:

$$K = \nu e^{-h\nu/kt}$$

and it can be shown that this relation also holds for K calculated from (1). K is of the order of 10^{13}.

Bibliography

SEITZ F. (1940) *The Modern Theory of Solids*, New York: McGraw-Hill.

JUNCTION, HYBRID. A hybrid junction is a type of four-terminal microwave bridge circuit. It is named after the well known hybrid coil, or transformer, used for duplex telephone communication. Its performance as a circuit is closely analogous to that

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MULTI-FUNCTION VIDEO LINE BUFFER

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Preliminary Information

MULTI-FUNCTION VIDEO LINE BUFFER

Features

- Stores 1024 Words of 10 bits
- One Line and Two Line Configurations
- Programmable Line Lengths: 64, 128, 256, 512, 1024
- Intermediate Line Lengths by Truncation
- Delay Line and Sequential Access Modes
- Three 10 bit Parallel Data Ports: Input, Input/Output, and Output
- Cascadable to Increase Word Width, Line Length, and Number of Lines Stored
- Internal Address Generation
- 50 ns Cycle Time
- TTL Compatible I/O
- Fully Static Low Power CMOS/SOS Implementation

Applications

- Tapped Two Line Delay for 3 x 3 Filters
- Row to Column Scan Conversion for Separated 2D Filters
- Sequential Access Memory
- Support Chip for 1D/2D Convolver and Rank Order Filter

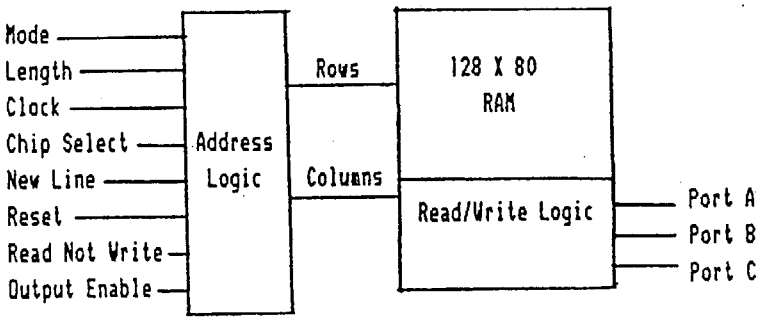
Description

The Multi-Function Video Line Buffer can be used as a tapped line delay or as a two dimensional sequential access memory. In the delay mode, one input port and two output ports provide a total delay of up to 1024 pixels, with a tap at half the length. In the sequential access mode, there is one X (row) port and there are two Y (column) ports. Image rows written to the X port may be read from the Y port as columns, and columns written to the Y port may be read from the X port as rows.

In all modes, the line length may be programmed to 64, 128, 256, 512, and 1024 pixels. Intermediate line lengths may be obtained by truncation on four word boundaries. Line lengths of 512 and less provide two lines of storage.

The Mode input selects Delay, X to Y or Y to X configurations and the Length input programs the natural line length. Reset initialises the pointer to the first pixel of the first line. Each pixel access is synchronous with Clock, which is enabled by Chip Select; Read Not Write determines the data direction. New Line steps the pointer to the first pixel of the next line, to facilitate truncation if required. Output Enable controls bus access from the output ports.

The two Y ports access two pixels per cycle, providing twice the peak data rate of the X port. This allows a full 20 M samples per second subsystem throughput in separated 2D Rank Order Filter applications.



This product is in development; specifications are subject to change.

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DESIGN RULES FOR STANDARD LINEWIDTH MEASUREMENT STRUCTURES

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DESIGN RULES FOR STANDARD LINEWIDTH MEASUREMENT STRUCTURES

1. SCOPE

To provide Applicon file locations, design details, and correct use of the obligatory standard linewidth structures for the following processes:

S1	C1
S1.5	C1.5
S2	C2.5
S3	C2.5 (DLM)
S5	C1.5 (DLM)
	C1.0 (DLM)

2. STATUS

This is a LETTER ISSUE document, denoting INTERMEDIATE STATUS.

3. RELATED DOCUMENTS

See section 4.

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4. FILE LOCATIONS

ALL AT APPL2::DNϕ:[3ϕϕ,1ϕϕ]

PROCESS	DESIGN RULES	QSI REFERENCE	APPLICON FILE LOCATION
S1	NOT ISSUED	--	USE S1.5 TARGET
S1.5	WORKING	DR 156(W) ISS.A	LINES15W.CEL
S1.5	Target	DT 156(T) ISS.B	LINES15T.CEL
S2	WORKING	DR 145(W) ISS.B	LINES2W.CEL
S2	Target	DT 145(T) ISS.B	LINES2T.CEL
C1.0	WORKING	DT 271 Draft a	LINEC10W.CEL
C1.0	TARGET	DT 271 Draft a	LINEC10T.CEL
C1.5	WORKING	DR 167(W) ISS.A	LINEC15W.CEL
C1.5	Target	DT 167(T) ISS.B	LINEC15T.CEL
C2.5	N/A	DR 139 ISS.B	LINEC25.CEL
C1.0 DLM	WORKING	DT 271 Draft a	LINEC10DW.CEL
C1.0 DLM	TARGET	DT 271 Draft a	LINEC10DT.CEL
C1.5 DLM	WORKING	DR 211(W) ISS.A	LINEC15DW.CEL
C1.5 DLM	Target	DT 211(T) ISS.A	LINEC15DT.CEL
C2.5 DLM	N/A	DR 144 ISS.A	LINEC25D.CEL
S3	N/A	DR 133 ISS.D	LINES3.CEL
S5	N/A	DR 157 ISS.A	LINES5.CEL

5. CORRECT CHOICE AND SUGGESTED LOCATIONS OF STANDARD LINEWIDTH STRUCTURE CELL

5.1 A standard linewidth structure cell IS OBLIGATORY with ALL OF THE ABOVE PROCESSES.

5.2 The linewidth cell design should be employed AS INDICATED BY THE ABOVE TABLE

5.3 If the design employs a mixture of working and target rules then the DEFAULT OPTION for the linewidth cell IS WORKING RULES.

5.4 Possible locations for the linewidth cell (see fig 1) are:

a. In the scribe channel, within a 'window' as shown by "E"
b. In other extremity positions, see "A", "C", or "F"
c. For test chips, in the main part of the die (but near the edge) see "B" or "D".

NOTE

1. The cell should always be located midway along the die (as shown) in order to maximise the consistency at the TRE imaging. Furthermore this minimises effects of poor resolution by ensuring the cell is as close as practically possible to the centre of the lens field.

2. The cell should also incorporate a 10μ perimeter of clear field to minimise proximity effects and the inconsistencies these may induce.

6. REQUIREMENT FOR STANDARD LINEWIDTH STRUCTURE CELLS

6.1 Linewidth readings from an optical measurement system are affected by structure characteristics OTHER THAN LINEWIDTH ITSELF. These characteristics can be classed as "design induced" (eg. proximity of linewidth structure to another structure) or "process induced" (eg. varying height, reflectivity etc.).

6.2 The design induced imprecision can be many times the tolerance required in the above processes. Standard linewidth cells are expected to eliminate this problem.

6.3 Process variations are to some extent dependant on the designed shape, size, position etc. of a structure. The standard linewidth cells hence help to minimise imprecision in data from this source also.

6.4 Note, the above imprecision is a PHYSICAL PROBLEM DUE TO OPTICAL PHENOMENA. It is unrelated to the "machine" precision and can only be evaluated via higher resolution measurements (eg. SEM).

7. DESIGN RULES EMPLOYED FOR CELLS

7.1 Cells are designed to provide the following;

a. Minimum design linewidth structures only
b. "Clear field" and "crowded filed" versions of these structures. The crowded field option employs minimum design separation of structures.
c. Contact (or via) holes as well as contact (or via) "lines".
d. The device relevant layer combination as well as further options.
e. Maximisation of structure symmetry for the available space.

7.2 The dimensions used, other than linewidth and spacewidths are as follows:

a. Minimum separation between unrelated structures, a structure and field edge or neighbouring field edges = 10µm.
b. Maximum width of cell maintained along whole of cell.
c. Length of crowded field line structure = 25µm, length of clear field line structure = 25µm.

8. EXAMPLE DESIGN

8.1 The cell to be used for C1.5 DLM WORKING RULES is taken as an example and the Applicon hardcopy included in this document (fig 2).

Fig. 1 General Arrangement For Accomodation of Linewidth Cell in 'Window' in Scribe Channel

Some Possible Locations for the Linewidth Structure Cell

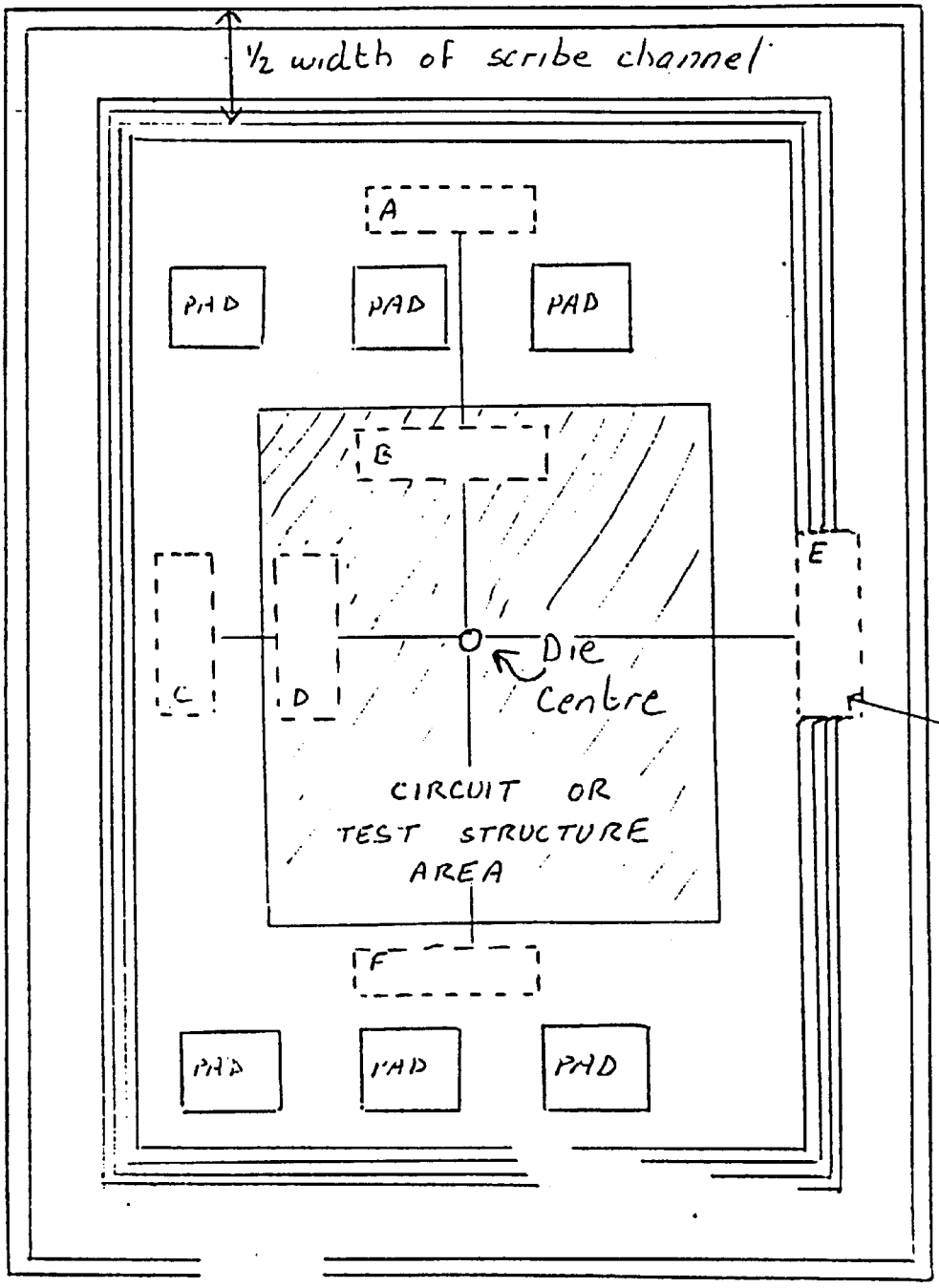


Fig ①

NOT TO SCALE

≡ Linewidth Structure Cell INCLUDING 10μ PERIMETER OF CLEARANCE.

break in perimeter ie/ cell area is equivalent to device area.

Fig. 2a C1.5 DLM Working Rule Example

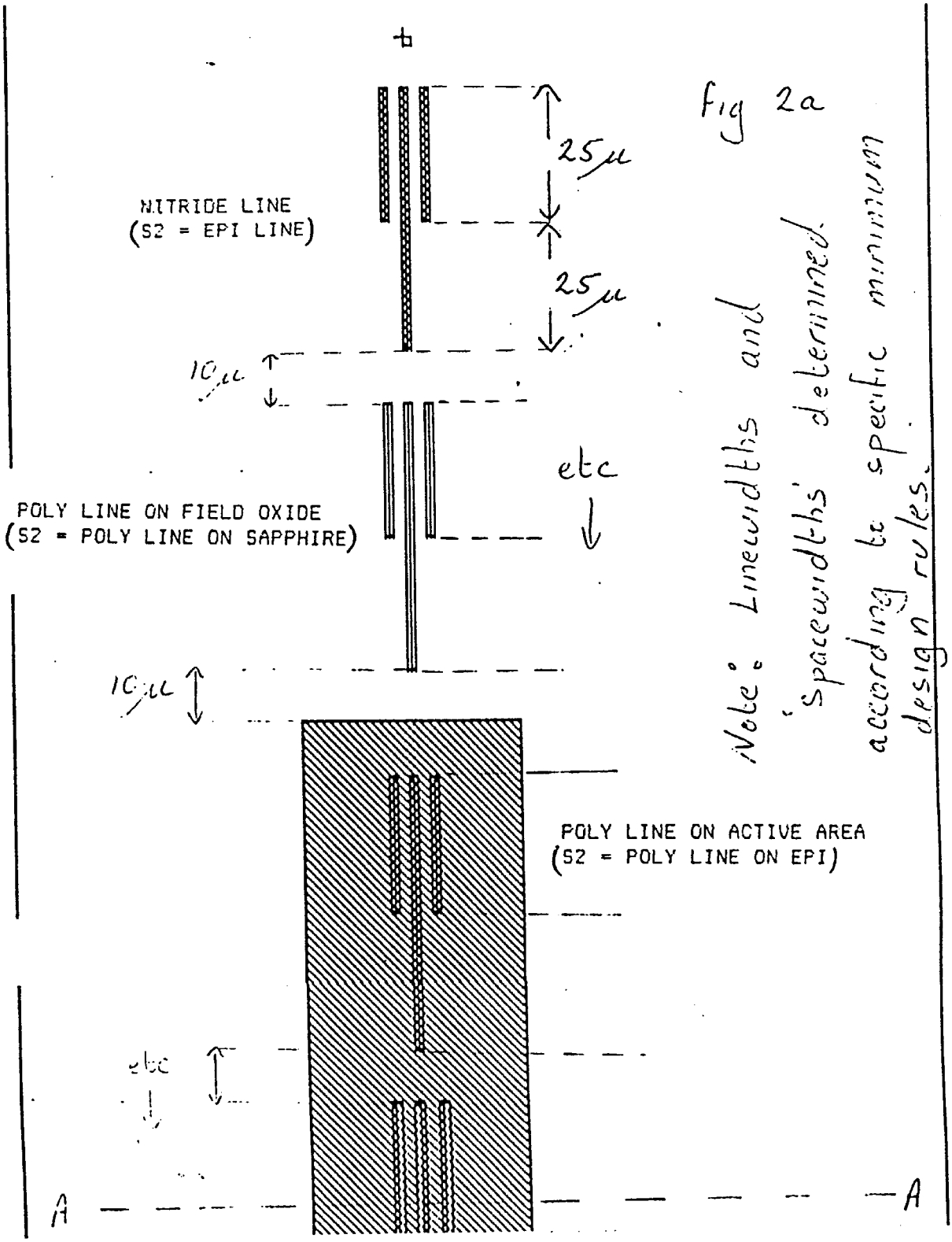
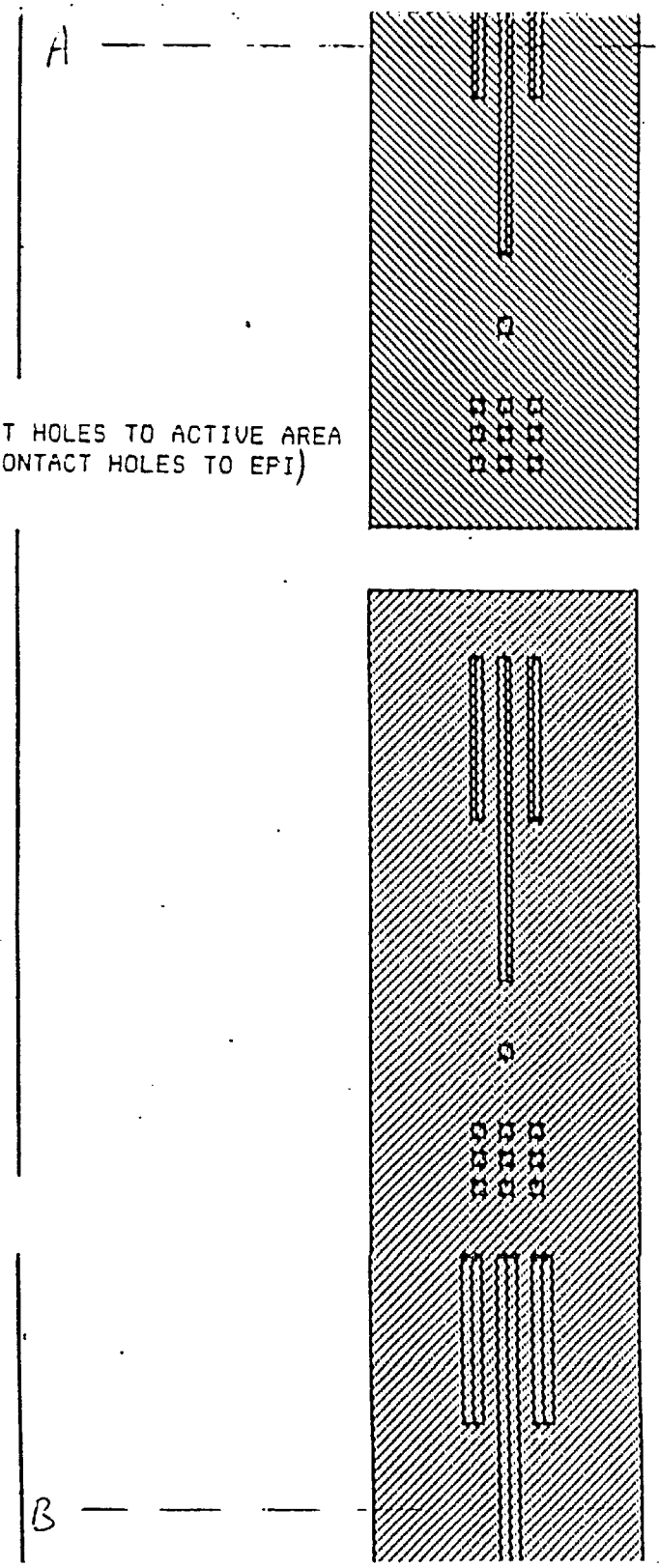


Fig 2a

Note: Linewidths and spacewidths determined according to specific minimum design rules.

Fig. 2b C1.5 DLM Example Continued



CONTACT LINE (ie: no vapox) TO ACTIVE AREA
(S2 = CONTACT LINE TO EPI)

CONTACT HOLE TO ACTIVE AREA
(S2 = CONTACT HOLE TO EPI)

CONTACT HOLES TO ACTIVE AREA
(S2 = CONTACT HOLES TO EPI)

Fig 2b

CONTACT LINE TO POLY ON FIELD OXIDE
(S2 = CONTACT LINE TO POLY ON SAPPHIRE)

CONTACT HOLE TO POLY ON FIELD OXIDE
(S2 = CONTACT HOLE TO POLY ON SAPPHIRE)

CONTACT HOLES TO POLY ON FIELD OXIDE
(S2 = CONTACT HOLES TO POLY ON SAPPHIRE)

METAL (I) LINE ON VAPOX OVER-
-POLY ON FIELD OXIDE
(S2 = METAL (I) LINE ON VAPOX-
OVER POLY ON SAPPHIRE

Fig. 2c C1.5 DLM Example Continued

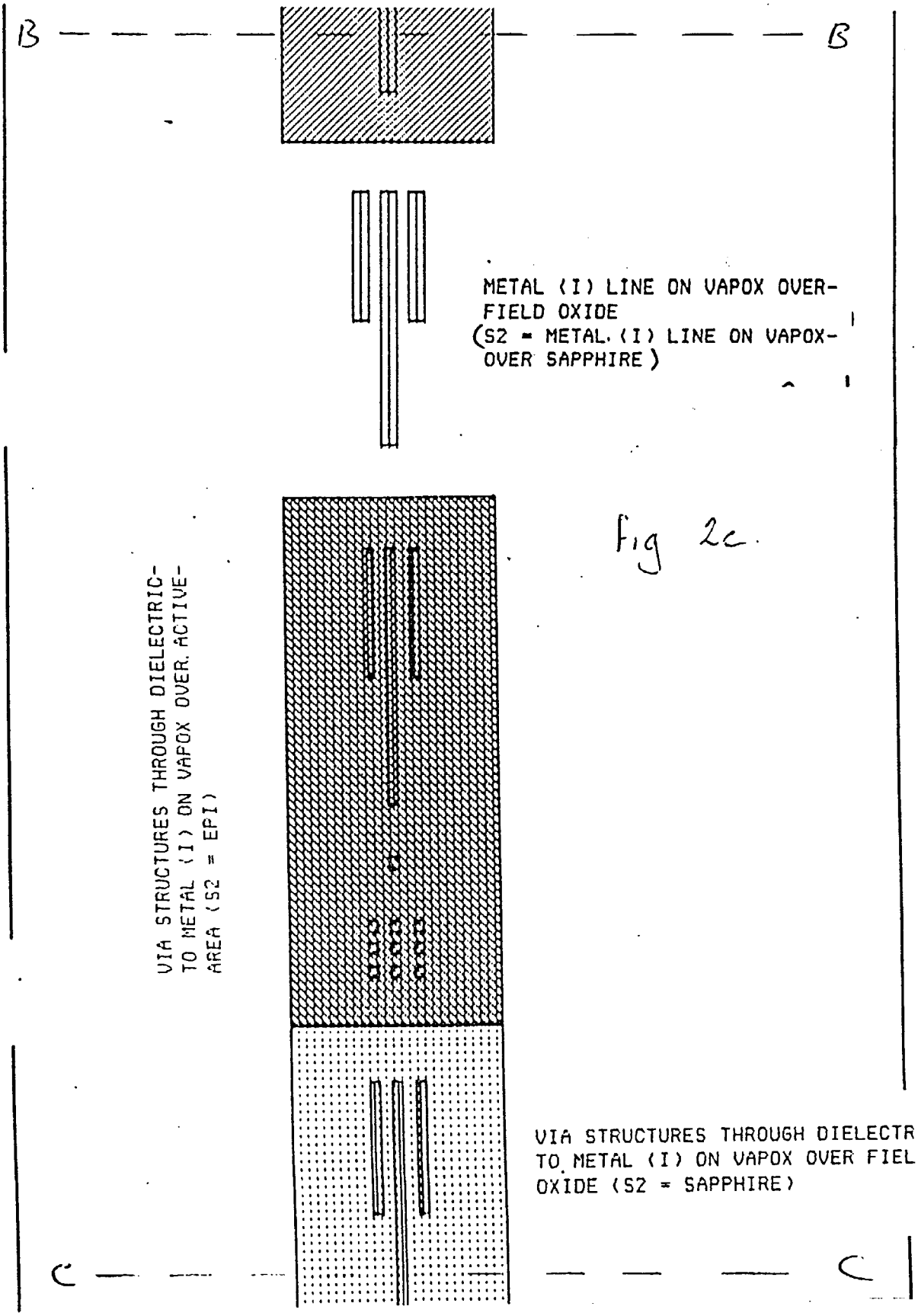
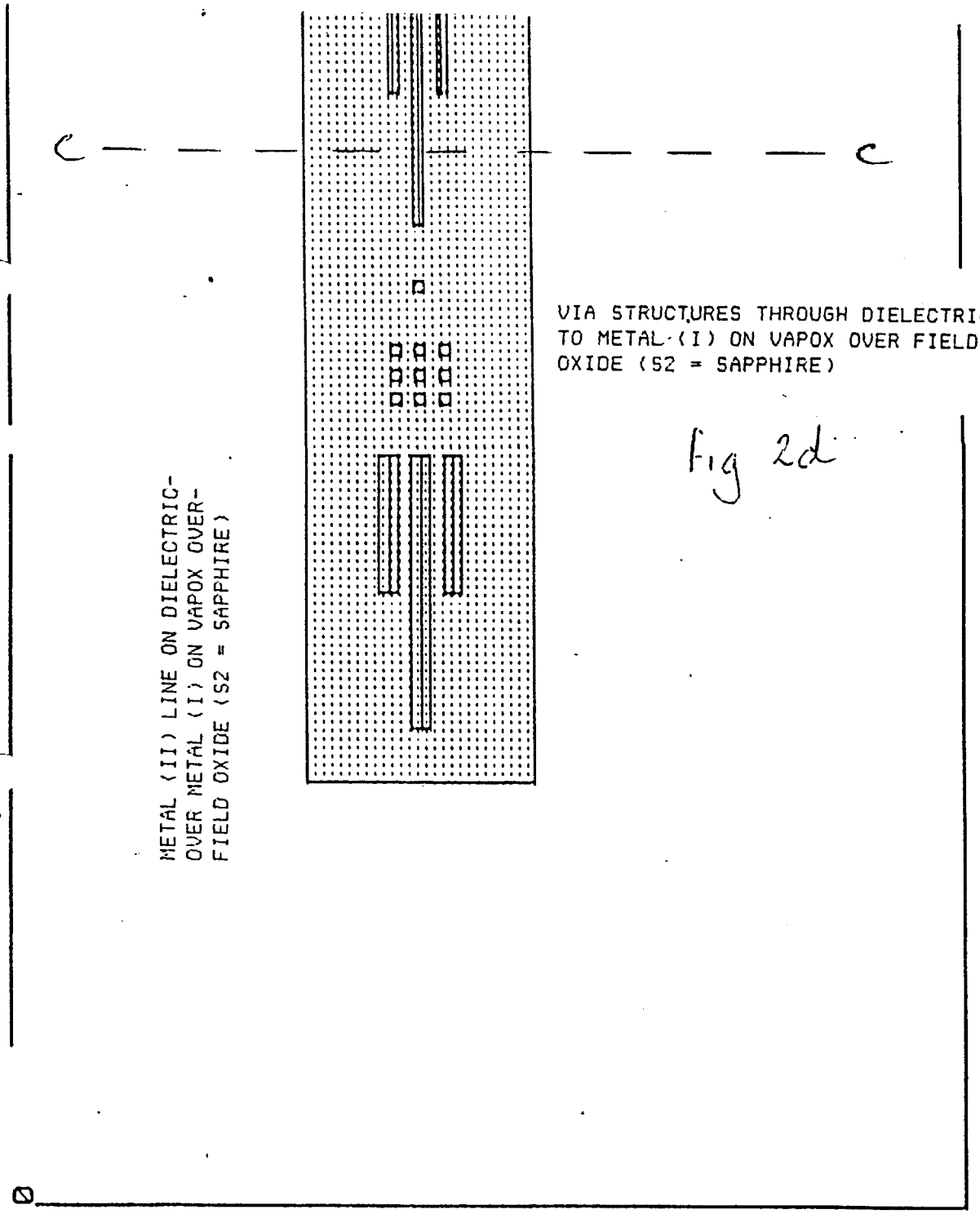


Fig 2c.

Fig. 2d C1.5 DLM Example Continued



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QSI-CD 250
(SILICON)

ISSUE: B

DATE: Midnight, Sunday
November 2nd, 1986

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49. S5 PE log
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52. R+D log
53. E Campbell
54. M Toothill

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CD SPECIFICATION SYSTEM COPY NO

1. SCOPE

1.1 To make operators' application of current specifications as error free as possible.

1.2 To allow ready and precise revision of specifications by all parties involved.

1.3 To document clearly all relevant data and maximize its accessibility.

2. STATUS

This is a LETTER ISSUE document, denoting INTERMEDIATE STATUS.

3. RELATED DOCUMENTS

3.1 Mask Biasing and Tolerancing	QSI-DR 135
3.2 OSI Measurement Procedure	QSI-MO 201

4. SYSTEM

4.1 To make Operators' Application of Current Specifications as Error Free as Possible

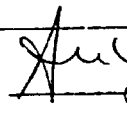
4.1.1 The CD engineer is responsible for ensuring the OPERATOR CD LOG is accurately updated in line with this QSI document.

4.1.2 The operator will apply simple minimum and maximum specifications entered in the operator's log by the CD engineer.

4.2 Definition of CD Specifications

4.2.1 CD specifications are specific to the mask design, layer and structure type (resist/etched) in question.

The TARGET CD to be aimed for is defined by the measured mask CD and the assumed process linewidth losses (ie: photolith and etch).

APPROVED FOR DISTRIBUTION  QL

CN NO:- 215

The minimum and maximum specifications are defined by the target CD and the appropriate TOLERANCES (±) allowed to either side of target.

The process linewidth losses and tolerances form the SPECIFICATION PARAMETERS which are tabulated in this document.

4.2.2 CALCULATION OF TARGET CD

Target Resist CD (Tr) = Measured Mask CD (M) - Resist Loss (P)

Target Etch CD (Te) = Measured Mask CD (M) - Total Loss (L)

Where: Total Loss (L) = Resist Loss (P) + Plasma Loss (E)

4.2.3 CALCULATION OF MINIMUM/MAXIMUM SPECIFICATIONS

Minimum Resist Spec (Rmin) = Target Resist CD (Tr) + Lower Resist Tolerance (rt-)

Maximum Resist Spec (Rmax) = Target Reist CD (Tr) + Upper Resist Tolerance (rt+)

Minimum Etched Spec (Emin) = Target Etched CD (Te) + Lower Etched Tolerance (et-)

Maximum Etched Spec (Emax) = Target Etched CD (Te) + Upper Etched Tolerance (et+)

Where: All underlined specification parameters are tabulated in this document.

4.2.4 NOTE (1): The total process linewidth loss may differ in magnitude from the mask bias due to the following:

a. Unsuitable mask bias, ie: an OLD bias mask is being run on a new process otherwise the present process losses or mask biases need revising.

b. A post-etch step is responsible for linewidth loss, eg: loss of active area width is due mainly to field oxide growth - NOT the photolith or etch steps.

4.2.5 NOTE (2): The "resist" and "plasma" losses may include losses due to other steps, eg: contact hole reflow at hardbake causes a reduction in linewidth. This consequently reduces the value of the resist loss parameter.

4.3 To Allow Ready and Precise Revision of all Specifications by all Parties Involved

4.3.1 Revision of specification parameters may only be accomplished via a "REVISION TABLE".

This table will provide a comparison of the new proposed parameters with the parameters presently in force.

4.3.2 The revision table must clearly define the criteria on which the new parameters are based.

Any data employed for this must be quoted. Furthermore, a full list of all the relevant batches and the period over which the CD measurements were taken is required.

4.3.3 The proposed parameters will come into force upon the associated change note being correctly signed off in the usual manner.

4.3.4 The vetoing of individual parameters must be accompanied by full reasons (and relevant data) along with an alternative value.

The vetoing of certain parameters will not prevent issuing of non-vetoed parameters.

4.3.5 The SQ engineer will revise parameters, as above, on a 3 monthly basis.

4.4 To Document Clearly all Relevant Data and Maximize its Accessibility

4.4.1 The parameter revision table, once signed off, will become the vehicle for current specification parameters.

4.4.2 A copy of the operator's log will be held by the SQ and CD engineers.

This will contain details of designed CD's, biases, etc pertaining to a particular mask set/layer/structure combination. See example sheet on page 4.

4.4.3 It is vital for many parties normally remote from the cleanroom activities and data to be able to make an accurate assessment of "concessed" batches. This requires that all relevant data is included in concessions for linewidth measurement steps.

The operator who raises a concession is therefore responsible for including the following information:

a. Concession serial number

b. Date raised

c. Batch number

d. Batch originator

e. Process (eg: S2, S3TRE etc)

f. Step code (eg: 45/MO etc)

g. Layer (eg: metal (I), poly etc)

h. State whether resist or etched measurement

i. Full design title AND issue (or QC) number

j. Measured mask CD

k. Ordered mask bias

l. Designated CD size (ie as drawn)

m. Target CD

n. Minimum spec

o Maximum spec

p. A clear entry of measured CD sizes obtained such as to identify different dies and wafers, viz:

Enter wafer number before each set of readings for a wafer. Enter the individual die readings IN THIS ORDER ONLY: C, N, S, E, W.

eg: (wfr1) 2.46, 2.47, 2.48, 2.47, 2.46 (wfr10) 2.56, 2.54, 2.56, 2.57, 2.54 (wfr17) 2.45, 2.46 etc, etc.

4.5 Responsible Personnel

4.5.1 CD Engineers: S A Haws, D Talks, D Kent, P Varsani, W J O Boyle, A E Adams

4.5.2 SQ Engineer: J Abbess

4.6 Change Note Authorisers/Vetoers (for future spec revisions)

4.6.1 Authorisers: CD and SQ engineers and A H Nott ONLY.

4.6.2 Vetoers: D W Tomes, D G Barlow, N Samarakone, D Talks, L W Kennedy, E Read, D E H Smith, H J Dedic, A Frier - AT LEAST.

5. TABLES OF CURRENT SPECIFICATION PARAMETERS

5.1 Resist and plasma loss parameters are as agreed at CD specification meeting of 17/9/86.

5.2 Resist and etched (final) tolerances are as agreed at above meeting.

5.3 The parameters included in the tables are listed below.

"P" - Resist linewidth loss

"E" - Plasma linewidth loss

"L" - Total Process loss ie: P+E

"rt+" - Upper resist tolerance

"rt-" - Lower resist tolerance

"et+" - Upper etch tolerance

"et-" - Lower etch tolerance

NOTE: ALL DIMENSIONS ARE IN µm

LINEWIDTH LOSS PARAMETERS, DETERMINING TARGET CD LINEWIDTHS FROM MASK SIZE
TRE PROCESSES, PROPOSED VALUES

		TECHNOLOGY					
LAYER	LOSS	S3	S2	S1.5	S1.0	C1.5	C1.0
EPI OR NITRIDE	RESIST PLASMA TOTAL	+0.20 1.00(317) +1.20	+0.20 +.20(804) +0.40	+0.20 +.20(804) +0.40		+0.20 +.20(804) +0.40	
POLY	RESIST PLASMA TOTAL	+0.20 +.60(425) +0.80	+0.20 +.20(804) +0.40	+0.20 +.20(804) +0.40		+0.20 +.05(804) +0.25	
CONTACT	RESIST PLASMA TOTAL	-0.20 -.15(425) -0.35	-0.20 +.10(903) -0.10	-0.20 +.10(903) -0.10		-0.20 +.05(903) -0.15	
METAL I	RESIST PLASMA TOTAL	+0.45 .00(425) +0.45	+0.45 .00(425) +0.45	+0.45 .00(425) +0.45		+0.45 .00(425) +0.45	

LINEWIDTH TOLERANCES, DETERMINING MIN AND MAX CD SPECS FROM TARGET SIZE
TRE PROCESSES, PROPOSED VALUE

		TECHNOLOGY					
LAYER	LOSS	S3	S2	S1.5	S1.0	C1.5	C1.0
EPI OR NITRIDE	Resist	+/-.30	+0.1,-0.2	+0.1,-0.2		+0.1,-0.21	
	Etched	+/-.50	+0.2,-0.3	+0.2,-0.3		+0.2,-0.3	
POLY	Resist	+/-.25	+/-.15	+/-.15		+/-.15	
	Etched	+/-.30	+/-.20	+/-.20		+/-.20	
CONTAC	Resist	+/-.30	+/-.20	+/-.20		+/-.20	
	Etched	+/-.35	+/-.30	+/-.30		+/-.25	
METAL I	Resist	+/-.30	+/-.30	+/-.30		+/-.30	
	Etched	+/-.40	+/-.40	+/-.40		+/-.40	

LINEWIDTH LOSS PARAMETERS, DETERMINING TARGET CD LINEWIDTHS FROM MASK SIZE
NON TRE PROCESSES, PROPOSED VALUES

		TECHNOLOGY					
LAYER	LOSS	S5 CANON	S5 PERK. L.	S3 PERK. L.	C2.5 PERK. L.		
EPI OR NITRIDE	RESIST PLASMA TOTAL	-0.60 +.90(317) +0.30	-0.90 +.90(317) 0.00	+0.20 +.30(317) +0.50	+0.20 +.20(317) +0.40		
POLY	RESIST PLASMA TOTAL	-0.60 +.60(425) 0.00	-0.90 +.60(425) -0.30	+0.20 +.60(425) +0.80	+0.20 +.35(425) +0.55		
CONTACT	RESIST PLASMA TOTAL	+0.60 -1.00(WET -0.40	+0.90 -1.00(WET -0.10	0.00 -.25(425) -0.25	0.00 -.15(425) -0.15		
METAL I	RESIST PLASMA TOTAL	-0.60 +2.00(WET +1.40	-0.90 +2.00(WET +1.10	+0.20 +.00(425) +0.20	+0.20 +.00(425) +.20		

LINEWIDTH TOLERANCES, DETERMINING MIN AND MAX CD SPECS FROM TARGET SIZE
NON TRE PROCESSES, PROPOSED VALUES

		TECHNOLOGY					
LAYER	LOSS	S5 CANON	S5 PERK. L.	S3 PERK. L.	C2.5 PERK. L.		
EPI OR NITRIDE	Resist	+/-.30	+/-.30	+/-.20		+/-.20	
	Etched	+/-.50	+/-.50	+/-.30	.	+/-.20	
POLY	Resist	+/-.30	+/-.30	+/-.20		+/-.25	
	Etched	+/-.50	+/-.50	+/-.30		+/-.30	
CONTACT	Resist	+/-.40	+/-.40	+/-.20		+/-.30	
	Etched	+/-.60	+/-.60	+/-.30		+/-.35	
METAL I	Resist	+/-.40	+/-.40	+/-.30		+/-.30	
	Etched	+/-.60	+/-.60	+/-.40		+/-.40	

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QSI-PS 298 ISSUE A DATE MARCH 1987

PROCUREMENT SPECIFICATION FOR 100mm DIAMETER SILICON ON SAPPHIRE WAFERS

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PROCUREMENT SPECIFICATION FOR 100mm DIAMETER SILICON ON SAPPHIRE WAFERS

1. SCOPE

This instruction is the procurement specification which must be quoted when ordering 100mm diameter silicon-on-sapphire wafers. Copies to be sent to HRC approved suppliers (except page four). It was prepared by T B Peters.

2. STATUS

This is a LETTER issue document denoting INTERMEDIATE status.

3. RELATED DOCUMENTS

Inspection document for SOS wafers.

4. SPECIFICATIONS

SAPPHIRE SUBSTRATE

DIAMETER	100±0.25mm
THICKNESS	0.53±0.05mm
TAPER	20microns Max
BOW	50microns Max
FLATNESS	10 microns Max unless ordered to a tighter specification.
FLAT WIDTH	30-35mm
FLAT LOCATION	45 ± 2 degrees to the projected 'c' axis

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PROCUREMENT SPECIFICATION FOR 100mm DIAMETER SILICON ON SAPPHIRE WAFERS

ORIENTATION	Within 2 degrees of the $(1\bar{1}02)$ "r" plane
SLIP, TWINS	None allowed
EDGE CHIPS	No more than 5 chips per substrate. 90% of the substrates shall have no chips greater than 1mm deep and 6mm long. All chips to be bevelled.
PURITY	Metallic impurities shall be less than 200 PPM as determined by emission spectrograph.
DISLOCATION DENSITY	Not to exceed 10^5 dislocation/cm^2 as determined by chemical etching.
SUBSTRATE SCRATCHES	See criteria and inspection method for epi film.
BACK SURFACE FINISH	0.8 microns CLA
EDGE CONTOUR	Both sides bevelled.
WAFER FLAT LINEARITY	The wafer shall be inspected by ASTM method F671-83 or a similar technique and shall be linear to within ± 150 microns maximum deviation. Any convexity or concavity shall be included in this measurement and specification.

EPITAXIAL LAYER

FILM THICKNESS	0.6 microns ±10%) 0.4 microns ±10%)To be specified on 0.3 microns ±10%)order
FILM TYPE	Intrinsic
RESISTIVITY	Greater than 100 ohm.cm as measured with a four point probe.

VISUAL DEFECTS (Pits, non removable surface particules)(>2 microns)	To be specified on order
HAZE	Heteroepitaxial silicon layer to be free of haze as determined by glancing angle reflected light test.
ULTRA VIOLET REFLECTANCE	Centre point 280nm reflectance values to be included in the quality control inspection prior to shipment and the values included with the certificate of conformance. None of these readings should exceed 40 units.
SURFACE FINISH	No scratches greater than 12mm are allowed with a total length of 50mm for all scratches. 90% of the wafers shall have no scratches. Inspection method shall be with a bright light in a darkened room.

5. PACKAGING AND GENERAL

a. Wafers to be packed in boxes of 25 wafers with each box labelled with Manufacturer, Lot Number, Date of Fabrication or Shipping, Epitaxial Layer Thickness, Thickness Uniformity Specification, Flatness.

b. Sites of growing, sawing, lapping and polishing to be declared by the manufacturer.

c. Certificate of conformance is required.

d. The epitaxial reactor to be specified.

6. APPROVED SUPPLIER

Kyocera Corporation

U.K Agent
Feldmuhle Kyocera Europa
Elektronische Bauelemente GmbH
26 Hemmells
Laindon North Trade Centre
Laindon, Essex
SS15 6ED

Production Plant
Kyoto Ceramic Co Ltd
52-11 Inoue-cho, Higashino
Yamashina-ku, Kyoto 607
Japan

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100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

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100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

1. SCOPE

This document is the procurement specification which must be quoted when ordering 100mm epitaxial wafers for C1.0. Copies to be sent to HRC suppliers.

2. STATUS

This is a LETTER ISSUE document, denoting INTERMEDIATE STATUS.

3. RELATED DOCUMENTS

4. SPECIFICATION

SUBSTRATE

TYPE/DOPANT	p-type: boron
RESISTIVITY	10-20 mohm cm To be determined by procedure ASTM F672
CRYSTAL GROWTH	Czochralski
RADIAL RESISTIVITY VARIATION	To be specified To be determined by procedure ASTM F672 on agreed sampling plan
ORIENTATION	<100> ± 1°
OXYGEN CONTENT	Not specified
CARBON CONTENT	Not specified
HEAVY METAL CONTAMINATION	5ng/g max. To be determined by atomic absorption.
PRIMARY AND SECONDARY FLATS	Locations to follow SEMI specification M1-85 and dimensions to follow SEMI Std M1 STD. 5-85

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100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

EPITAXIAL LAYER

TYPE/DOPANT	p-type: boron
RESISTIVITY	To be specified on order To be measured by spreading resistance ASTM F672
RADIAL RESISTIVITY VARIATION	12% max
DOPING GRADIENT	The tranisition width between 90% of the epitaxial layer resistivity to 110% of the substrate resistivity is to be no greater than 1µm. To be determined by ASTM F 672
THICKNESS	5µm ± 7.5% To be determined by procedure ASTM F672
VISUAL INSPECTION OF SURFACE	Conditions according to ASTM F523 (1983)
SCRATCHES	At least 97% of all wafers to be free from scratches
HAZE	None
DIMPLES	10/wafer max
ORANGE PEEL	None
PARTICULATES	97% of all wafers to be free from particulates and the remainder to have no more than 3/wafer
EDGE CHIPS	2/wafer max
EDGE CROWNING	$^1/_3$ max of epi thickness
STACKING FAULTS	5/cm^2 To be determined by procedure ASTM F522 (1978)
SLIP	None

100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

SPIKES	3/wafer max To be determined by procedure ASTM F815 (1983). Spikes not to be removed.
DEFECT DENSITY	To be determined by procedure outlined in ASTM F80-85
DISLOCATION ETCH PITS	100/cm^2 max
HEAVY METAL CONTAMINATION	Less than 5ng/g in the total epi layer
OXIDATION INDUCED DEFECTS	As determined by test method outlined in ASTM F416 (1984) with modified conditions as follows:

Insertion Temperature	850 °C
Ramp Rate	10 °C/min
Anneal	60 mins in dry nitrogen
Oxidation	950 °C in steam 420 mins
Withdrawl	10 °C/min to 850 °C

FINISHED WAFER

THICKNESS	525 ± 25 mic + epi layer
DIAMETER	100 ± 0.05mm
BOW	40µm max
TAPER	40µm max
SURFACE FLATNESS	3µm max

BACKSIDE

Unless otherwise specified the backside is to be caustic etched. IF backside damage is required it will be fully specified on the order.

SAW MARKS	None
WORK DAMAGE	None

100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

PACKAGING AND GENERAL

1. Wafers to be vacuum packed in 25 wafer lots.
2. Sites of growing, sawing, lapping and polishing to be declared by the manufacturer.
3. Certificate of conformance is required.
4. The epitaxial reactor must be specified.

HRC QUALITY (SILICON)	REFERENCE NO QSI-PS 296	ISSUE A	DATE FEB 87	PAGE 5 OF 5

100 mm P-TYPE EPITAXIAL WAFERS FOR CMOS

APPROVED SUPPLIERS

Wacker Chemicals

U.K Agent
The Clock Tower
Mount Felix
Bridge Street
Walton-on-Thames

Production Plant
Wacker-Chemitronic GmbH
P O Box 1140
D-8263 Burghausen
West Germany

On Wacker orders specify

BACKSIDE

Wacker proprietary "Brush" damage to be present on backside of wafers.

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QSI-DS 239 ISSUE: Draft a DATE: APRIL 1986

SIGNAL STREAM Product Family

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Preliminary Information

SIGNAL STREAM

Product Family

FEATURES

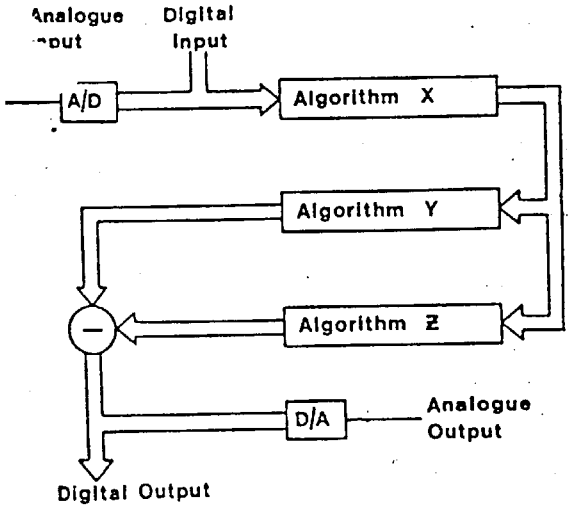
* Comprehensive set of building blocks for signal stream data processing
* High level of integration to reduce part count
* High speed - family supports 20Msample/sec data rates
* High computational throughput by use of pipelining and systolic array techniques
* Low Power CMOS-SOS technology
* Family includes the:

  Bit-slice Correlator
  1/2-D Convolver
  Rank Order Filter
  Multi Function Video Line Buffer
  Cascade - ALU

* Cascadable to extend sizes of blocks or to implement compound algorithms

APPLICATIONS

* Real time image processing
* Real time radar processing
* Digital radio
* Image/signal processing workstations
* Computer graphics
* Embedded signal processing systems



GENERAL DESCRIPTION

Marconi Electronic Devices' Signal Stream family of devices provides all the major elements required in high speed digital signal processing. The family includes: a bit-slice correlator, a 1/2-D convolver, a rank order filter, a multi-function video line buffer and a cascade - ALU. These products will be used where the best available computational throughput is required from available technology, and will revolutionize low level signal processing by allowing to build real time algorithms from Signal Stream blocks.

Many applications such as low level image processing, radar signal processing and computer graphics require the processing of streams of data in real time. Conventional signal processors cannot match such data rates suggesting that novel architectures must be employed. Marconi's Signal Stream product family employs systolic array and pipelined architectures to allow very high data rates to be processed. Futhermore, the use of CMOS-SOS technology in these devices reduces the power consumption and dissipation in real time systems.

The Signal Stream concept provides a set of building blocks which are capable of performing operations on streams of data. The bit-slice correlator, 1/2-D convolver and rank order filter permit real time correlation, linear and non-linear filtering. Compound algorithms can be implemented by cascading several types of devices from the family including the line buffer and cascade - ALU support elements.

Signal Stream products have a high degree of integration and could considerably reduce the size of systems designed with first generation DSP circuits; for example a single 1/2-D convolver would replace 9 multipliers and several glue logic devices. The will allow reductions in part count and board space and make system design more straightforward.

Since the product family is optimised for processing long streams of data changes of system configuration are likely to be infrequent. In embedded applications such as front-end processors the processor instructions can be hardwired; alternatively in signal processing workstations the configuration of Signal Stream devices can be altered under microprogram control.

This product is in development; specifications are subject to change.

QSI-DS239
Version:a, Apr 86
Distribution:B

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MA 7188 CASCADE-ALU

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MA7188 CASCADE-ALU

ADVANCE INFORMATION

TURES

16-bit 20MHz ALU with programmable delay of 0-31 clock cycles on one input

16-function ALU
Add/subtract, absolute value, minimum/maximum selection
AND, OR, XOR, XNOR

Overflow, Zero and SGN flags - SGN flag can be used as 17th output bit

Cascadable for multiple-precison arithmetic at 20MHz and to extend the length of programmable delay

TTL compatible input/output

Fully static CMOS-SOS implementation

Standard 68-pin LCC package

APPLICATIONS

- Cascading MA7180 1-D/2-D convolvers to increase convolution window size and wordlengths
- Combining the outputs of two pipelined systems with the same throughput but different processing latencies
- Fast and low power word-wide ALU for digital signal and image processing applications

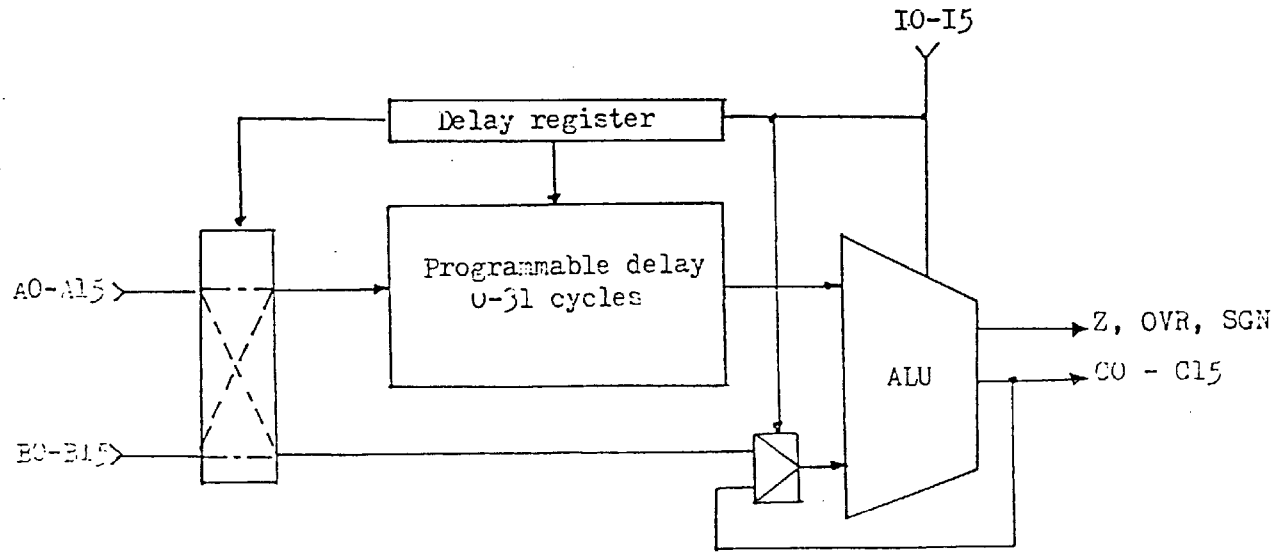
ASSOCIATED DEVICES

- MA7180 1-D/2-D Convolver
- MA7186 Video line buffer
- MA7190 Rank order filter

SCRIPTION

7188 is 20 MHz 16-bit arithmetic unit with two input ports A B and an output port C. One of the inputs can be delayed by to 31 clock cycles prior to ALU operation. This feature es the device very useful in compensating for the difference ween the latencies of two pipelined systems, before combining ir outputs. The length of the delay can be increased by scading MA7180 devices or by cascading MA7188 and MA7186. An ortant application of this latency compensation property is cascading MA7180 1-D/2-D convolver devices to increase the volution window size or the wordlengths.

The ALU supports commonly required arithmetic and logic functions. Novel ALU features include absolute value computation and the facility to select the larger or the smaller of the two input operands as the output. Arithmetic overflows can be overcome by using the right shift facility at ALU output or by taking the SGN flag as the 17th bit of the output. Multiple-precision arithmetic and composite arithmetic operations can be carried out in a single clock cycle using a cascade of devices or in several clock cycles using a single device.



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MA7188 DETAILED DESCRIPTION

MA7188 is a 16-bit 20MHz arithmetic logic unit. A programmable delay of up to 31 cycles can be applied to either input prior to ALU operation. This programmable delay is very useful for combining the outputs of two pipelined systems with the same throughput but different processing latencies. One of the main applications of this device is in cascading MA7180 1-D/2-D convolvers to increase the convolution window size beyond (3x3) or (1x9) and data and coefficient wordlengths beyond 10 and 12 bits. A functional block diagram of this device is shown in figure 1.

The ALU supports the commonly required arithmetic and logic functions. Two novel features of the ALU are absolute value computation and minimum/maximum value selection. The right shift facility is useful for preventing overflows. Alternatively, a 17-bit output can be obtained by using the ALU flag SGN as the 17th bit of the output. Multiple-precision (32-bit, 64-bit) arithmetic can be carried out by cascading devices, with no degradation in the throughput. Multiple-precision arithmetic can also be carried out using a single device in multiple cycles. Absolute value and min/max operations are restricted to 16-bit numbers. The ALU output can be re-cycled as one of the ALU input operands, allowing the implementation of composite operations such as P+Q using a single MA7188 device.

Data inputs, outputs and enabling signals

MA7188 has two 16-bit data input ports A0-A15 and B0-B15. The inputs are assumed to be two's complement numbers for arithmetic operations in the ALU.

The inputs A and B are registered on the rising edge of the CLK input, when the input enable signals IEA and IEB are LOW. The inputs A and B are disabled when IEA and IEB are HIGH. These inputs can be disabled only when the length of the programmable delay is zero. Both enable signals IEA and IEB must be held LOW when the length of the programmable delay is non-zero.

The data outputs C0-C15 and the three ALU flags Z, OVR and SGN are avaiable from registers. A new set of outputs will be available following the rising edge of the CLK input. When the output enable signal OE is HIGH the data outputs C0-C15 will be in a high impedence state. The ALU flags are not three-state outputs and are unaffected by the OE input.

Control registers CR, DR and IR

Three 6-bit control registers, Cascade control register CR, Delay control register DR and an instruction register IR, are provided to hold the programmable delay control, cascade control and ALU instruction control signals. All three registers are loaded from the 6-bit instruction input port I0-I5 on the rising edge of the CLK input as shown in figure 2. The register to be loaded is selected using the inputs SRLEN and IRLEN as given by table 2. Programmable delay and cascade control are static control signals and hence DR and CR can be loaded prior to system operation. After loading CR and DR the SRLEN input may be held HIGH so that the ALU instruction register can, if required, be updated every clock cycle under the control of the IRLEN signal.

The zero-delay and single-chip operating mode is given by zero values in the registers CR and DR (Details of the use of these registers are described later). These two registers can be reset to zero by holding the SRLEN and RST signals low for a period which includes the rising edge of the CLK input, as shown in figure 2.

Table 1 : Selecting control registers for loading

SRLEN	IRLEN	Control register selected
0	1	Programmable delay control register DR
0	0	Cascade control register CR
1	0	Instruction register IR
1	1	No control registers selected

Programmable delay control

The length of the programmable delay and the input (A or B) to be delayed are determined by the contents of the programmable delay control register DR0-DR5. The five bits DR0-DR4, interpretted as a binary number, specifies the length of the programmable delay in clock cycles. The bit DR5 specifies the input to be delayed. If DR5=0 A input is delayed and if DR5=1 B input is delayed.

The programmable delay has been implemented using a memory. Hence, after loading the register DR, it is necessary to ensure that this memory is correctly addressed. The simplest method of achieving this is to allow a system initialisation period of 32 or more clock cycles after loading DR and before loading the first data sample (see figure 3a). This relatively long system initialisation period can be avoided by using the RST input. In this method the first data sample must be loaded in the first clock cycle following the clock cycle in which is the system is reset by bringing RST LOW, as shown in figure 3b. Note that

this time in which RST is LOW should include at least one rising edge of the CLK input. It is assumed that the register DR has been loaded prior to bringing RST input LOW (The RST input does not reset the register DR if the SRLEN input is HIGH).

If the length of the programmable delay is N cycles the output of the programmable delay will be undefined for N cycles after applying the first data input. It is not possible to update the register DR whilst preserving the contents of the programmable delay. Hence the device has to be initialised, using any of the two procedures described above, every time the register DR is updated. Any of these procedures need not be followed if the length of the programmable delay is zero. The registers CR and IR can be updated without affecting the programmable delay operation.

Both input enable signals IEA and IEB must be held LOW when the length of the programmable delay is non-zero. The programmable delay is used for latency compensation in pipelined systems and hence input disabling cannot be used in this mode of operation. The input enable signals are useful only when the device is being used an ALU with the programmable delay length set to zero. The memory used in implementing the programmable delay can be unselected to save power(when the device is not in use) by holding both IEA and IEB signals HIGH. The memory is also unselected when the length of the delay is zero.

Cascade control

There are two methods for cascading MA7188 devices, namely, the registered carry method and the ripple-carry method. In the former method the carry input of one device is registered before it is applied to the next most significant device. This is a pipelining technique which allows the 20MHz throughput to be maintained. In the ripple-carry method, the carry output is not registered. Hence the throughput is reduced, but the processing latency remains unaffected. These two cascading techniques are controlled by the first four bits, CR0-CR3, of the CR register. The functions of these signals are given in table 2 and illustrated in figure 1. Examples of the use of these control signals for device cascading are shown in figure 9, 10 and 11. The signals CR4 and CR5 are used for testing.

Table 2: Functions of the cascade control signals

Control signal	Function
CR0	CR0 must be set to 0 for the least significant device and must be set to 1 for all other devices in the cascade. When CR0=1 CIN is taken as the carry input to the ALU. When CR0=0 the input CIN is disregarded by the ALU.
CR1	If CR1 is set to 1 an additional single clock cycle delay is introduced into the paths of the two operand inputs and the instruction input. If CR1 is set to 0 this additional single clock cycle delay is not introduced.
CR2	If CR2 is set to 1 an additional single clock cycle delay is introduced between the ALU output and the device output C. If CR2 is set to 0 this delay is not introduced.
CR3	If CR3 is set to 0 the carry output COUT is registered. If CR3 is set to 1 COUT is not registered.

ALU operation control

The ALU operations are controlled by the contents of the 6-bit instruction register (IR0-IR5). This register is loaded from the instruction input port I0-I5, on the rising edge of the CLK input, when the IRLEN input is LOW and the SRLEN input is HIGH (Refer to table 1 and figure 2).

The first four bits of the 6-bit instruction register (IR0-IR3) determine the ALU instruction as given in table 3. The ALU operations have been defined using internal ALU inputs P and Q since these may not directly correspond to the device inputs A and B.

Absolute value and min/max instructions are two novel features of this ALU. The min instruction selects the smaller of the two input operands as the output. The max instruction selects the larger of the two input operands as the output. For the min and max instructions the SGN flag indicates which of the two inputs has been selected as the output (Refer to the description of ALU flags).

Refering to table 3 it is observed that there are two add instructions and three subtract instructions. For add and subtract operations in category (b) the carry input is taken as the carry output of the previous operation. Hence these instructions are required only when performing multiple-precision arithmetic operations using a single cascade-ALU. The add and subtract instructions in category (b) must be applied in the second and subsequent cycles of this multiple-precision arithmetic operation. For example, to perform a 32-bit addition in two clock cycles using one MA7188, the instruction 1001 is carried out in the first cycle on the 16 l.s.b. inputs and the instruction 0111 is carried out in the second cycle on the 16 m.s.b. inputs.

For arithmetic operations and absolute value operations (categories (a) and (c) of table 3) the computation result is a 17-bit two's complement number. Hence the arithemetic unit of the ALU always generates a 17-bit result assuming that the two input operands are in two's complement format. This 17th bit of the ALU output is available to the user as the SGN flag. If the SGN flag and C15 are not identical the OVR flag will be set HIGH indicating the presence of an overflow. Overflow can be prevented by shifting the ALU output by one bit towards the least significant bit. IR4 controls this right-shift operation. If IR4=1 the 17-bit ALU output is right shifted by one bit and the OVR flag is set LOW. This right shift facility is valid only for arithmetic operations ((a), (b) and (c) of table 3).

IR5 is used to control the re-cycling of the ALU output to the input port Q of the ALU. If IR5=1 the output of the previous clock cycle will be used as input Q of the ALU. This facility is useful for performing composite arithmetic operations such as

P+Q in two clock cycles using a single device. In the first clock cycle (P+Q) is performed and in the next the absolute value of (P+Q) is obtained. It should be noted that the absolute value instruction is valid only for 16-bit operands. Hence it may be necessary to right shift (P+Q) before absolute value computation.

ALU flags

MA7188 cascade-ALU produces three status flags Z, OVR and SGN. These flags are available at output from registers, following the rising edge of the CLK input.

Z is the zero flag. A HIGH value on the Z flag indicates that all the ALU outputs are zero.

OVR is the overflow flag. A HIGH value on the OVR flag indicates the presence of an arithmetic overflow in the ALU output. Arithmetic overflows can be prevented using the right-shift facility described under ALU operation control. If a full precision 17-bit output is required SGN flag can be used as the 17th bit of the output.

SGN is the sign flag. The function of this flag depends on the ALU operation. For the ALU operations in categories (a), (b) and (c) the SGN flag is the 17th output bit of the ALU, assuming two's complement input operands. Hence this flag can be used to obtain the true comparison between two operands or to obtain a 17-bit output. For the min/max operations in category (d) of table 3, the SGN flag indicates which of the ALU inputs has been selected as the output. If SGN flag is HIGH the output is the P input and if SGN flag is LOW the output is the Q input.

Table 3: ALU Instruction set

	Instruction IR3	IR2	IR1	IR0	Operation	Comments
(a)	1	0	0	1	P + Q	Arithmetic operations
	0	1	0	0	P - Q	
	0	0	1	1	Q - P	
	1	0	0	0	P	
	0	0	1	0	-P	
	1	1	0	1	-Q	
(b)	0	1	1	1	P + Q	Carry output re-cyled internally as the carry input for next clock cycle.
	0	1	0	1	P - Q	
(c)	0	0	0	0	|P|	Absolute value instructions
	1	1	1	1	|Q|	
(d)	1	0	1	1	Min(P,Q)	Selects the smaller or the larger of the two input operands as the output.
	1	1	0	0	Max(P,Q)	
(e)	0	0	0	1	P OR Q	Logic operations
	0	1	1	0	P AND Q	
	1	0	1	0	P XOR Q	
	1	1	1	0	P XNOR Q	

PIN DESCRIPTION

A0-A15

16-bit data input.

A inputs are registered on the rising edge of the CLK input, when IEA is LOW.

B0-B15

16-bit data input.

B inputs are registered on the rising edge of the CLK input, when IEB is LOW.

IEA

Input enable for the A input.

Loading of A data inputs is enabled when IEA is LOW and disabled when IEA is HIGH. IEA must be held LOW when the length of the programmable delay is non-zero.

IEB

Input enable for the B input.

Loading of B data inputs is enabled when IEB is LOW and disabled when IEB is HIGH. IEB must be held LOW when the length of the programmable delay is non-zero.

I0-I5

6-bit instruction input port.

These inputs are used to load the instruction register IR, cascade control register CR and the programmable delay control register DR. The register to be loaded is selected using the inputs SRLEN and IRLEN, as given in table 1. The selected register is loaded on the rising edge of the CLK input.

SRLEN, IRLEN

CR, DR and IR control register load enable signals.

RST

Reset input.

The programmable delay control register and the cascade control register are reset to zero on the rising edge of the CLK input when both SRLEN and RST are LOW. RST is also used to reset the programmable delay unit as described under programmable delay control.

C0-C15

16-bit three-state data output.

These outputs are available from a register following the rising edge of the CLK input, provided the output enable input OE is LOW. When the OE is HIGH the outputs are in the high impedence state.

OE

Output enable control signal.

Z

Zero output flag.

This flag is HIGH when all 16 ALU outputs are zero. Z is available from a register following the rising edge of the CLK input.

OVR

Overflow output flag.

This flag is HIGH when there is an arithmetic overflow in the 16-bit output C0-C15. OVR is available from a register following the rising edge of the CLK input.

SGN

Sign flag or the 17th bit of the arithmetic unit output.

For the arithmetic operations ((a), (b) and (c) of table 3) this is the 17th bit of the two's complement ALU output. For min/max instructions this flag indicates which of the two input operands to the ALU has been selected as the output. If SGN is LOW then the output is P and if SGN is HIGH then the output is Q. SGN

flag is available from a register following the rising edge of the CLK input.

CIN

Unregistered carry input.

COUT

Carry output.

If the mode control bit CR3 is equal to 0 then COUT is available from a register following the rising edge of the CLK input. If CR3 is equal to 1 then COUT is an unregistered output.

CLK

System clock input.

CASCADE-ALU APPLICATIONS

Latency compensation

One of the main applications of the cascade-ALU is in latency compensation. If it necessary to combine the outputs of two pipelined systems with the same throughput but different latencies, the programmable delay in the cascade-ALU can be used to compensate for the difference in latencies, as indicated in figure 5.

Cascading MA7180 1-D/2-D convolvers

The cascade-ALU is very useful in combining the outputs of MA7180 devices for extending the convolution window size beyond (3x3) or (1x9) and data and coefficient wordlengths above 10 and bits. Figure 6 shows a 36-stage 1-D convolver designed using four MA7180 devices and three MA7188 devices. Figure 7 shows two possible configurations for a (9x9) 2-D convolver using MA7180, MA7186 and MA7188 devices. MA7186 is the video line buffer.

Fast ALU

The cascade-ALU can be used as a fast, low power, word-wide ALU. Absolute value and min/max instructions are particullarly useful in digital signal and image processing. The min/max instruction can be used for operations such as hard limiting shown in figure 8.

Multiple-precision arithmetic

Multiple-precision arithmetic can be performed using a single MA7188 device in multiple clock cycles or using multiple-devices in a single clock cycle. The former method makes use of the re-cycled carry facility and special add/subtract instructions given in table 3. It is important to note that the absolute value and min/max instructions are limited to 16-bit operations.

Multiple-device, multiple-precision MA7188 systems can be designed using registered-carry or ripple-carry cascade techniques. For 32-bit arithmetic, the former method allows the maximum 20MHz throughput to be maintained. A 32-bit registered carry ALU is shown in figure 9. To compensate for the delay of the carry bit from one device to another, data inputs and outputs must also be delayed appropriately. This is achieved using the cascade control signals CR0-CR3. The ripple-carry cascading technique results in a reduction in the throughput, but avoids any increase in latency (see figure 10). Both ripple-carry and registered carry techniques have been used in

the 64-bit ALU shown in figure 11. The input and output registers and the programmable delay are not shown in the figures 9, 10 and 11.

DC ELCTRICAL CHARACTERISTICS V_{CC} = 5V ± 10% T_A = -55°C to 125°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	HIGH-level input voltage	2.0	-	-	Volts	
V_{IL}	LOW -level input voltage	-	-	0.8	Volts	
V_{OH}	HIGH-level output voltage	3.5			Volts	V_{CC} = min ; I_{OH} = -0.4mA
V_{OL}	LOW -level output voltage	-	-	0.5	Volts	V_{CC} = min ; I_{OL} = 2 .0mA
I_{LI}	Input leakage current				µA	V_{CC} = max ; V_{in} = 0 to V_{CC}
I_{LO}	Output leakage current				µA	High Z ; V_{CC} = max , V_{out}= 0 to V_{CC}
I_{CC}	Operating power supply current				mA	Output open ; V_{in}= TTL voltage Max clock cycle
I_{CCQ1}	Quiescent power supply current				mA	$V_{in} > V_{IH}$ or $V_{in} < V_{IL}$
I_{CCQ2}	Quiescent power supply current				mA	$V_{in} > V_{CC}$ - 0.2V or $V_{in} < 0.2V$

Note : Typical value measured at V_{CC} = 5.0 V and T_A = 25°C

CAPACITANCE T_A = 25°C

Symbol	Parameter	Max	Unit	Conditions
C_{in}	Input capacitance Clock / Data and controls		pF	V_{in} = 0V
C_{out}	Output capacitance		pF	V_{out}= 0V

A.C. CHARACTERISTICS TA = -55°C to 125°C VCC = 5V + 10%

Symbol	Parameter	Min	Typ	Max
t_{CY}	Clock period			
t_{PW}	Clock pulse width			
t_S	Data A0-A15, B0-B15 set up time			
t_H	Data A0-A15, B0-B15 hold time			
t_{SI}	Instruction(I0-I5) set up time			
t_{HI}	Instruction(I0-I5) hold time			
t_{SR}	SRLEN, IRLEN and RST set up time			
t_{HR}	SRLEN, IRLEN and RST hold time			
t_C	Delay in C0-C15 output			
t_{CD}	Disable time for C0-C15 output			
t_{CE}	Enable time for C0-C15 output			
t_F	Output delay in Z, OVR and SGN flags			
t_{CDR}	Output delay for registered COUT			
t_{CDU}	Output delay for unregistered COUT			
t_{CIO}	Propagation delay from unregistered CIN to unregistered COUT			
t_{CI}	Minimum time for the unregistered CIN to set up, before the next rising edge of the CLK input, to ensure a valid output			

Note : A 30pF load has been used in the output delay measurements.

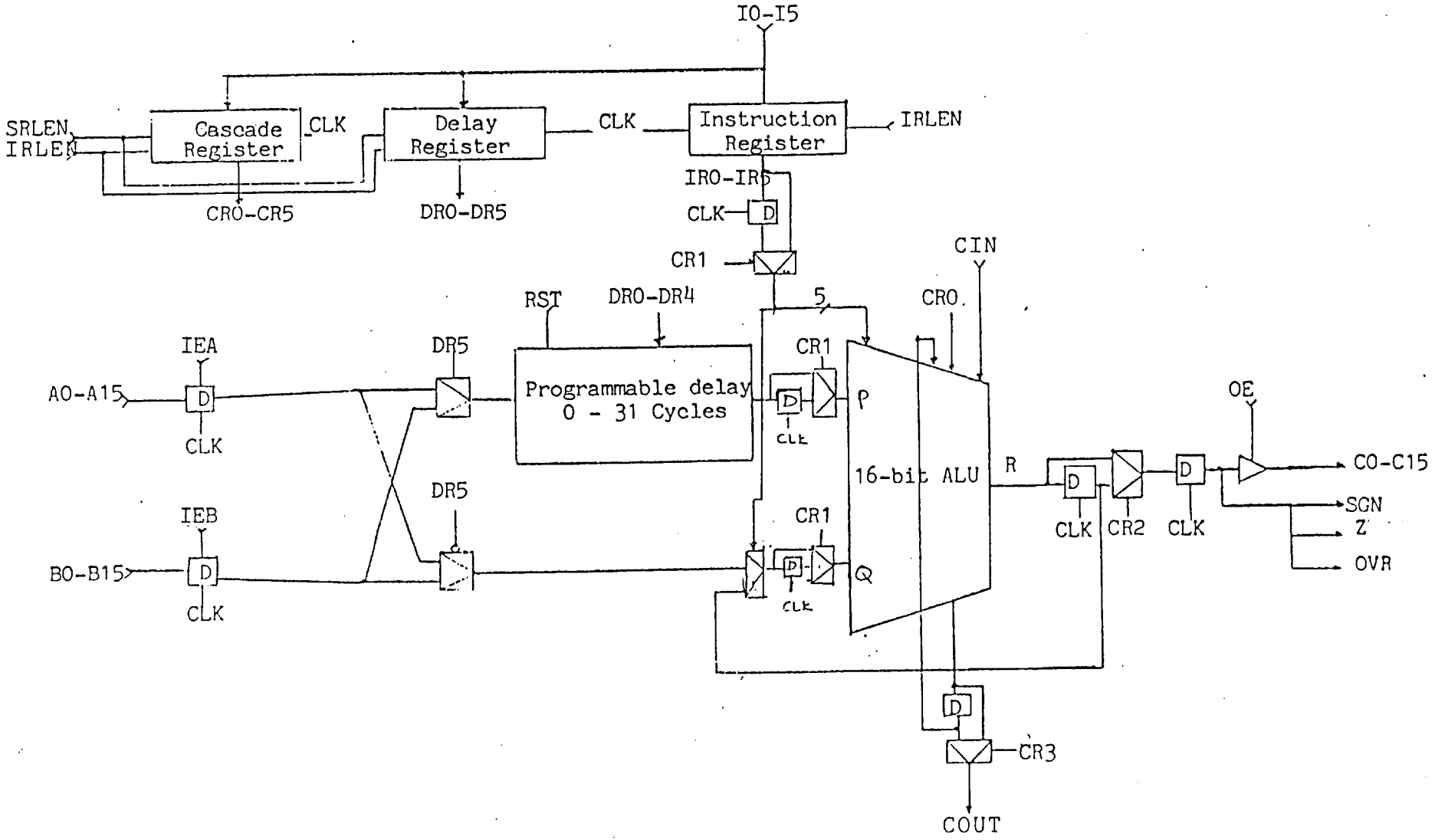


Figure 1 : Functional block diagram of MA7188 Cascade-ALU

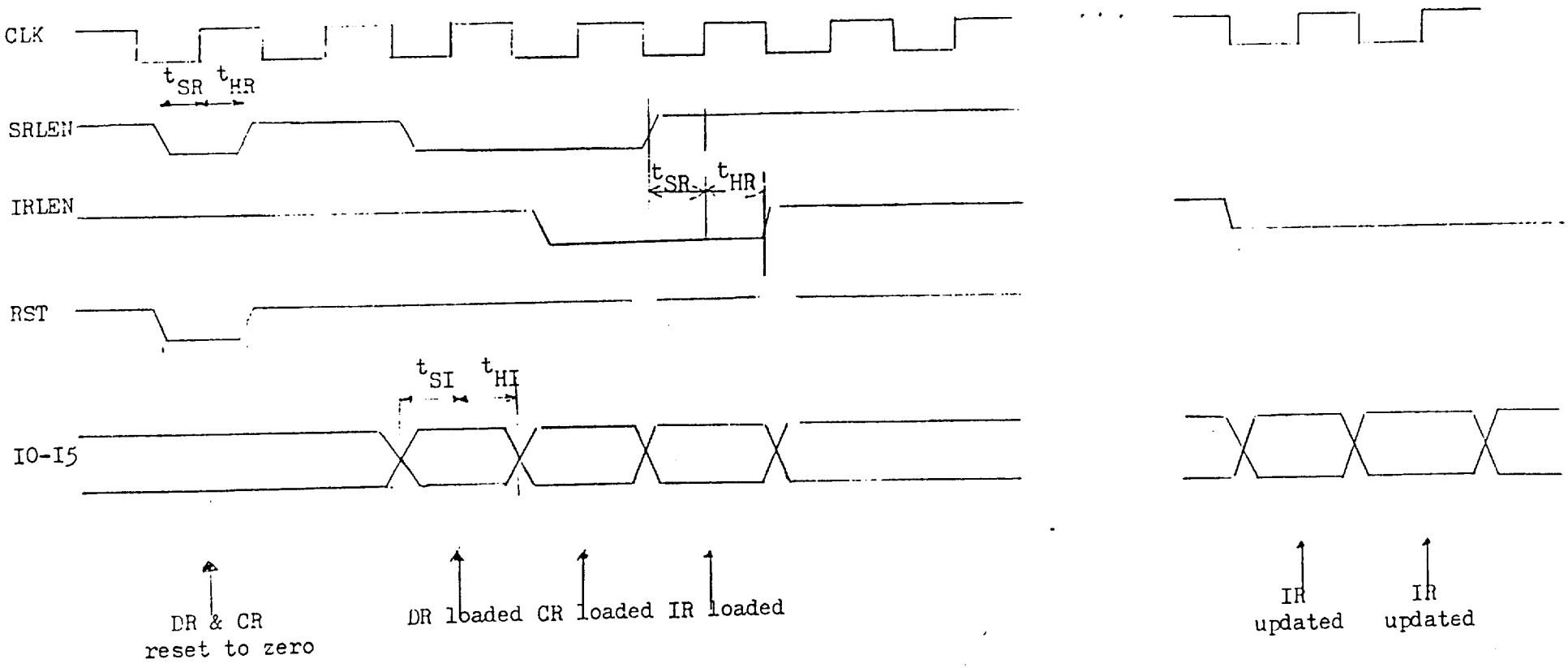


Figure 2 : Loading and updating control registers

DR .. Programmable delay control register CR .. Cascade control register IR .. Instruction register

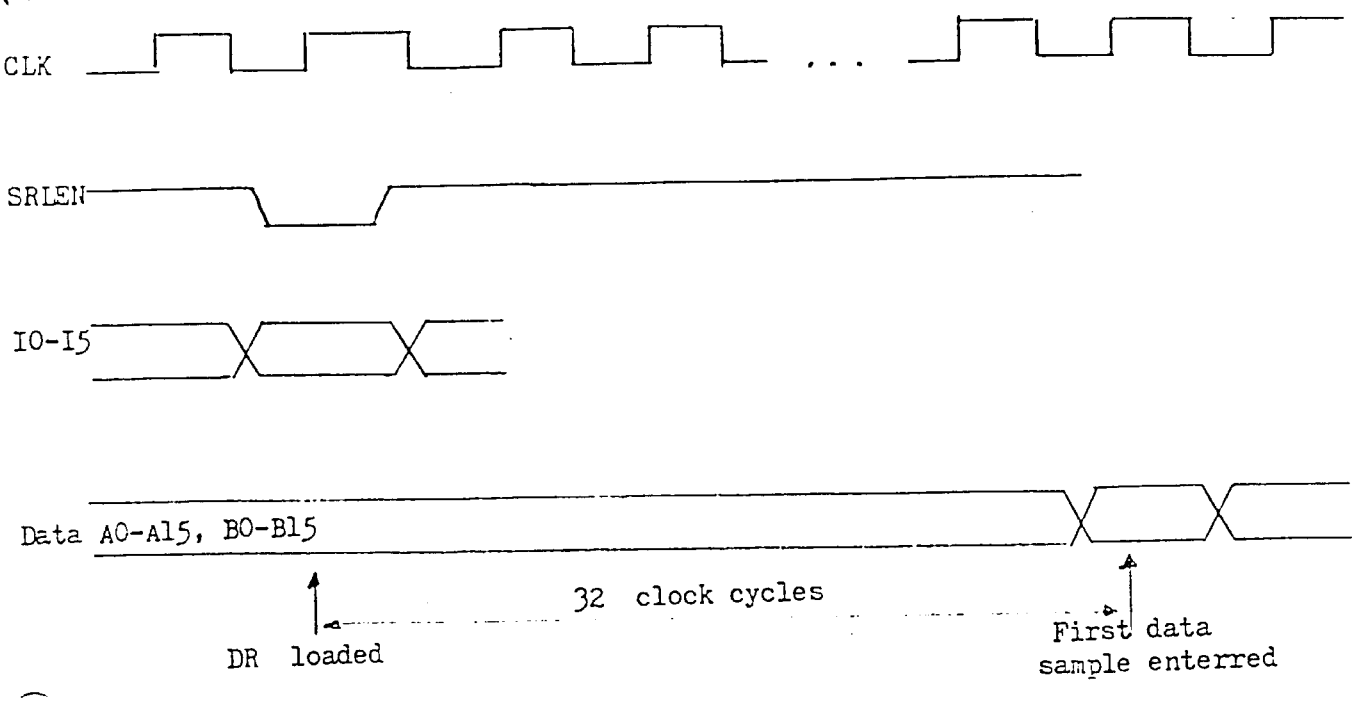


Figure 3a : Initialising the programmable delay unit (Method 1)

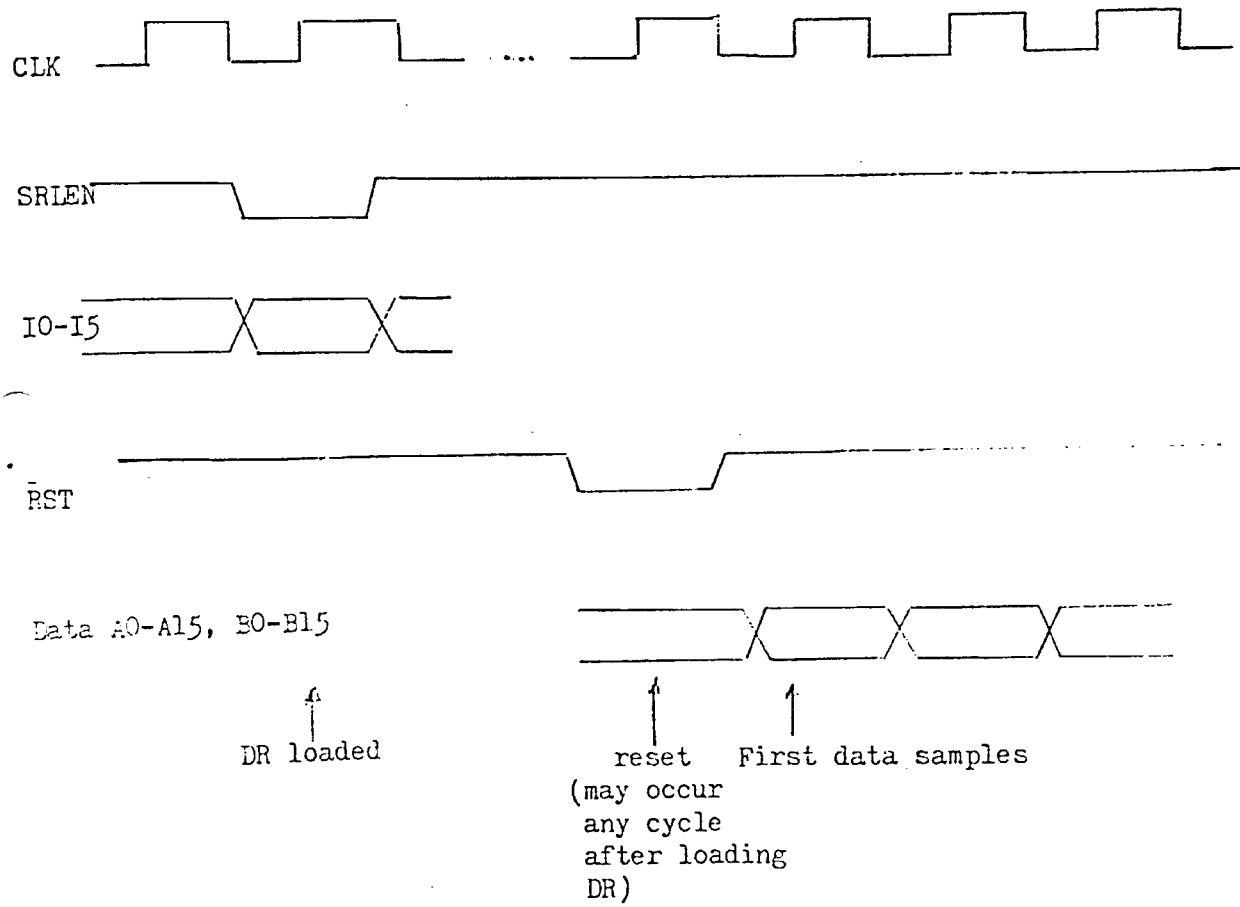


Figure 3b: Initialising the programmable delay unit (Method 2)

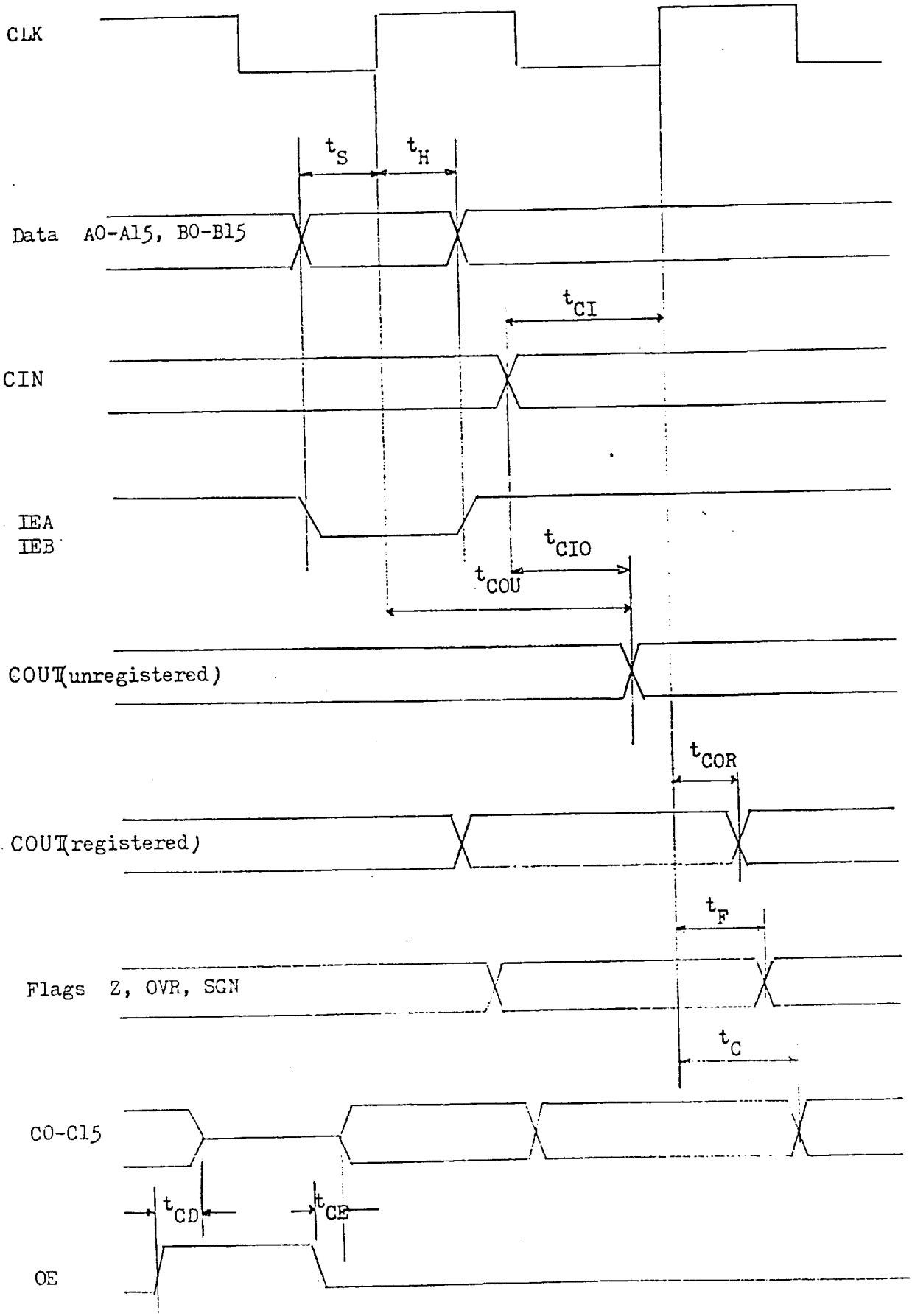
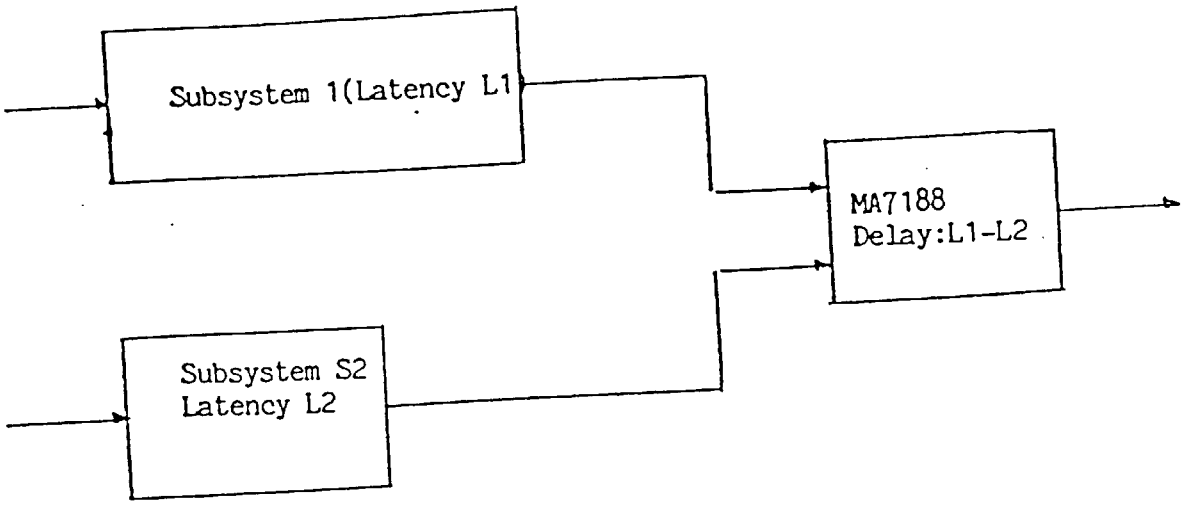


Figure 4: Timing diagram



Figue 5 : Use of MA7188 for latency compensation

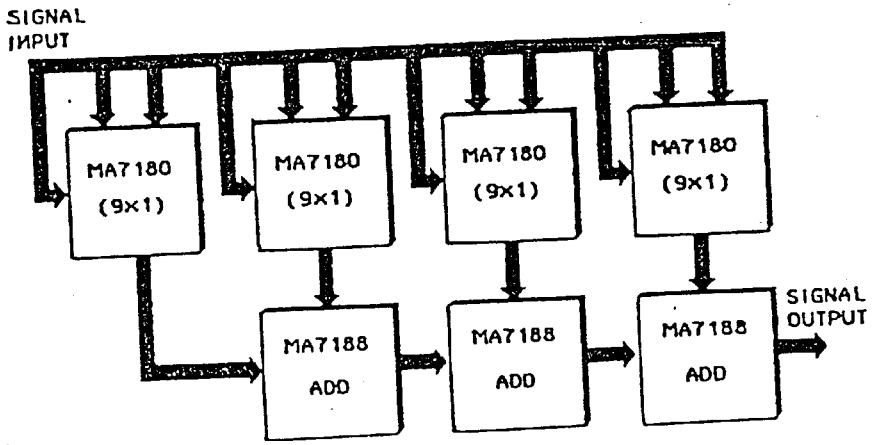


Figure 6: (36x1) CONVOLUTION

Figure 7a: (9x9) CONVOLVER SUBSYSTEM

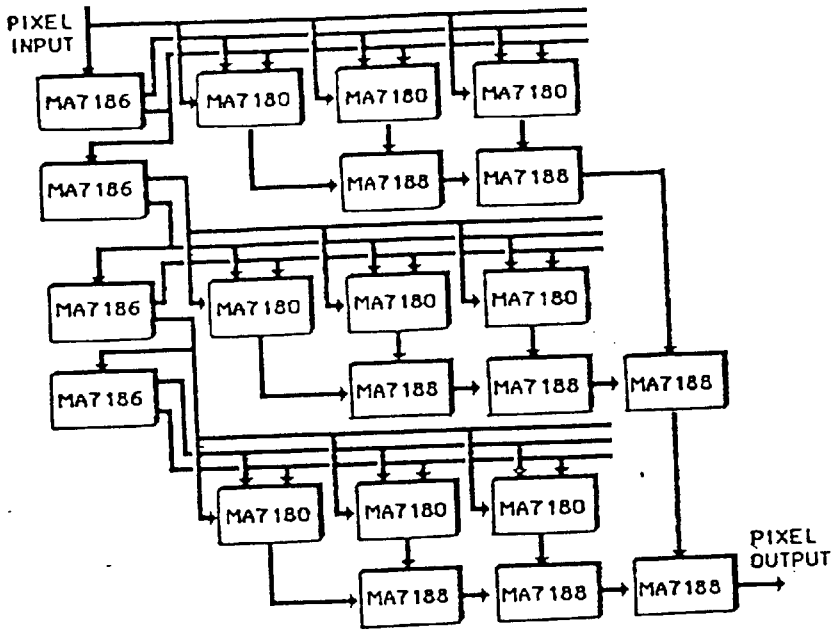


Figure 7b: ALTERNATIVE (9x9) CONVOLVER SUBSYSTEM

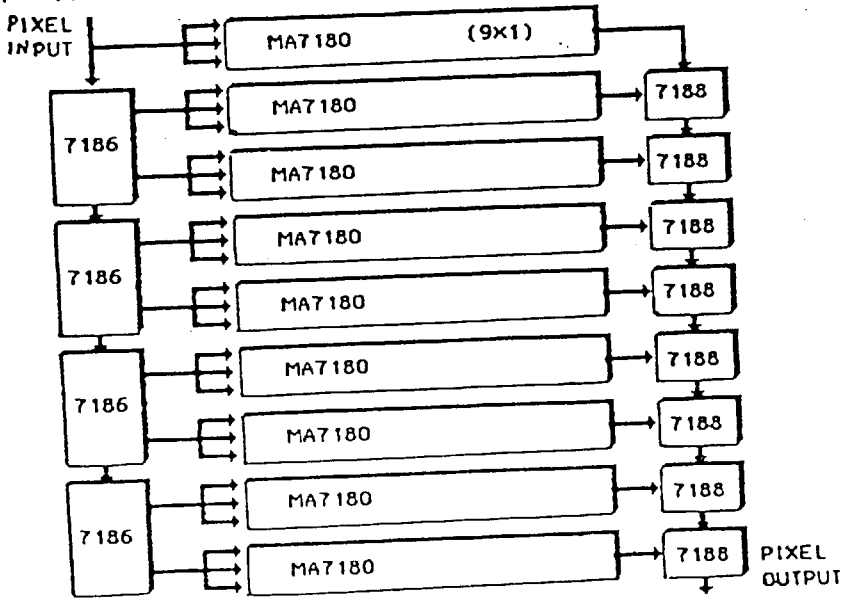
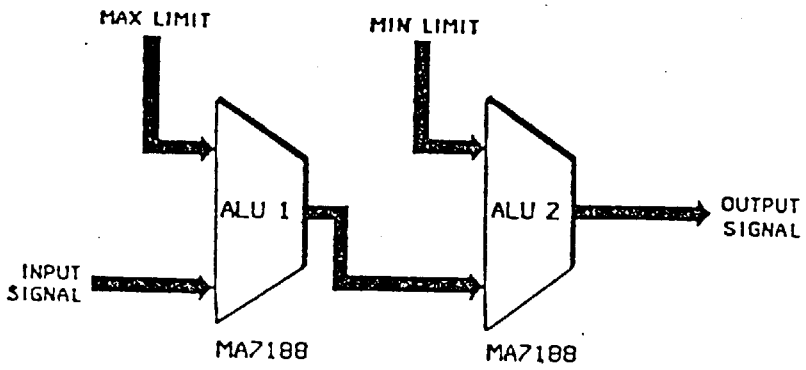


Figure 8: HARD LIMITING



ALU 1 SET TO MIN
ALU 2 SET TO MAX

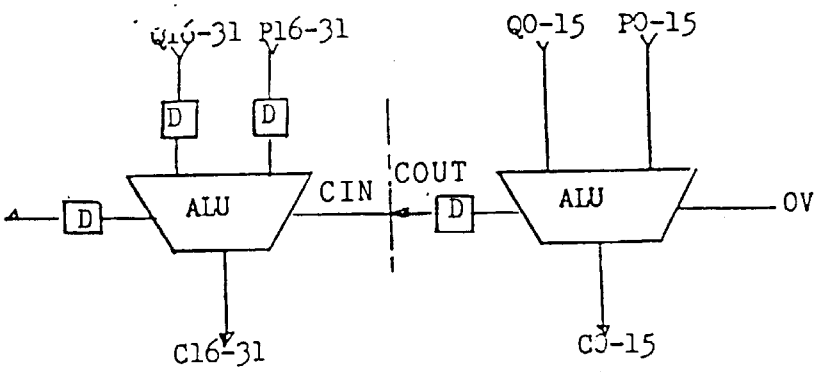


Figure 9 : Cascading MA7188 devices for 32-bit arithmetic using the registered carry method

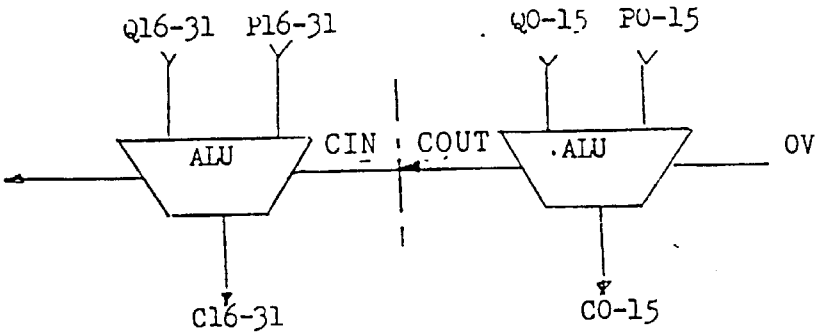


Figure 10: Cascading MA7188 devices for 32-bit arithmetic using the ripple carry method

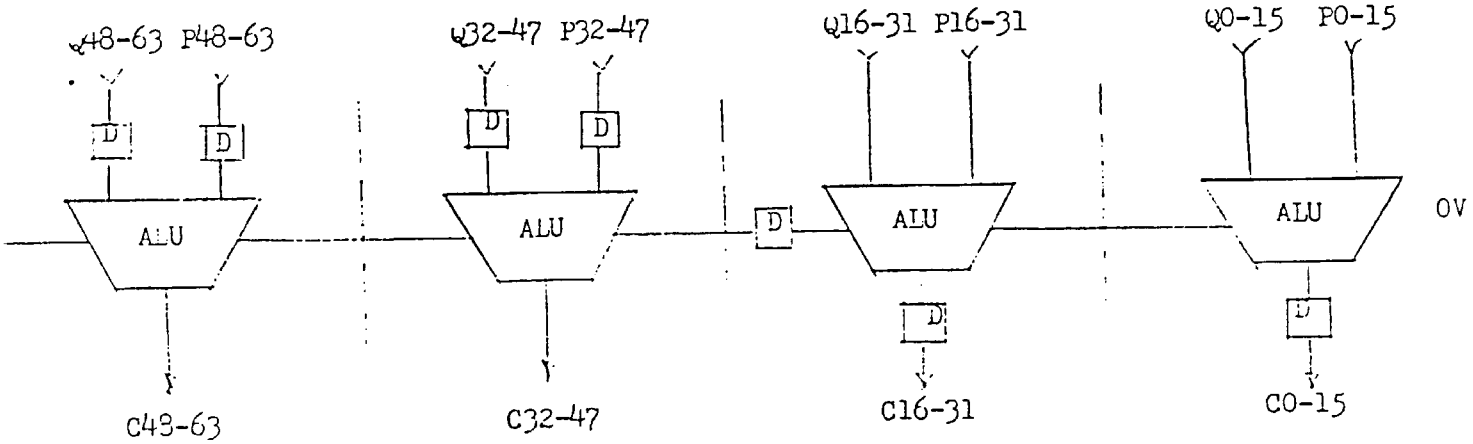
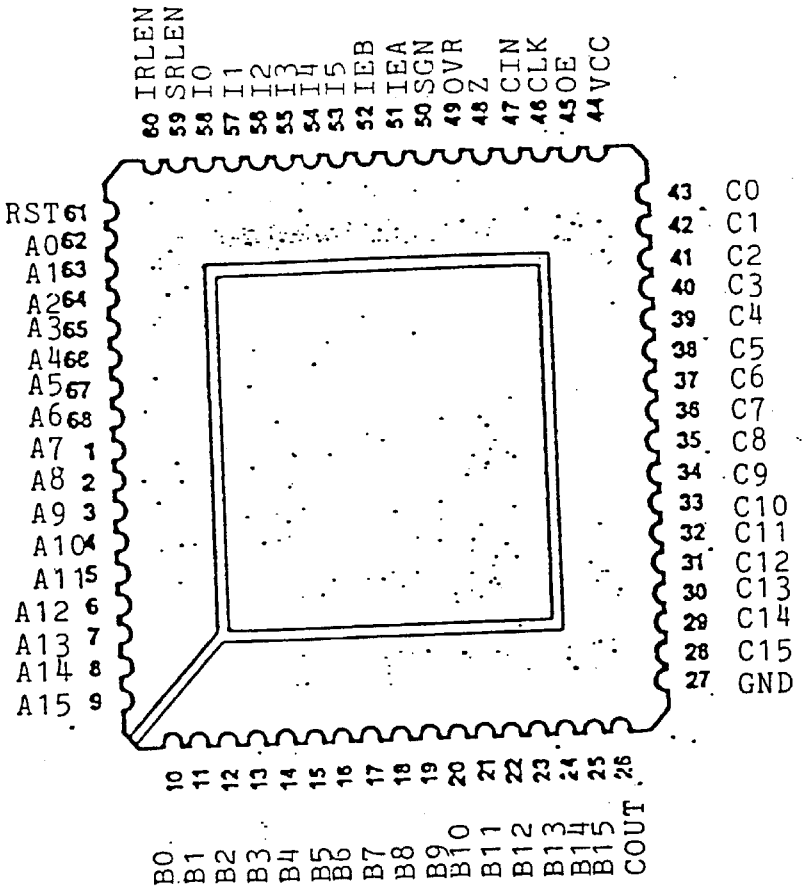


Figure 11 : Cascading MA7188 devices for 64-bit arithmetic using ripple-carry and registered-carry methods

Note : In figures 9, 10 and 11 the input registers, output registers and the programmable delay have not been shown.



MA7188 CASCADE-ALU

MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

Storage, Handling Precautions, Chip Mounting and Bonding Procedures

AN/102
Issue B
Sept 1987

APPLICATION NOTE

1. INTRODUCTION

This note offers guidance in the storage, handling, mounting and bonding of MMIC chips.

2. STORAGE

It is recommended that chips be stored in a clean, dry nitrogen environment until they are required for use.

3. HANDLING PRECAUTIONS

It must be emphasised that unmounted chips are extremely fragile and great care should be exercised at all times. Special care should be taken to avoid any contact with the exposed upper surface of the chips. It is recommended that the chips be handled by the edges, using a pair of flat-ended metallic tweezers. The usual precautions applicable to static-sensitive devices should be observed.

4. CHIP MOUNTING

To meet mechanical, electrical and thermal requirements the device must be correctly mounted on a gold-plated metallic base structure or carrier. The mount must provide secure physical support to the chip(s), both at assembly to allow thermocompression bonding of RF and DC wire connections, and in subsequent service.

Good electrical contact must be established and maintained between the metallised undersurface of the chip(s) and the plated attachment surface of the mount so as to realise fully the transmission line properties. This contact also provides a ground return for RF signals and DC supplies.

Signal input and output feeds in 50 ohm microstrip transmission line, and DC supply feeds, may be integral parts of the device mount, or may be points of an external circuit within which the carrier based chip(s) is fitted. In either case, the feeds should terminate in alignment with the appropriate chip pads to allow optimum interconnection.

4.1 Conductive Epoxy Mounting

Ablebond AB-58-1 gold loaded epoxy is recommended for conductive epoxy mounting. Apply a thin film of epoxy to the area of the carrier on which the chip is to be attached, leaving an epoxy-free border of approximately 0.5 mm inside the attachment area edges. Use epoxy sparingly to avoid migration up the sides of the chip or into via holes. The assembled carrier and chip should then be heated for 20 mins at 160°C to cure the epoxy adhesive.

4.2 Solder Mounting

Pure indium, or lead-indium-silver alloy (15/80/5) solder is recommended for conductive solder mounting. Heat the chip carrier to 160°C and apply a thin film of the selected solder to the area on which the chip is to be mounted. The placed chip and carrier should then be re-heated in an atmosphere of dry nitrogen, or forming gas, until solder attachment occurs at about 160°C. A solder flux is essential to ensure good, reliable adhesion; good wetting being achieved using a mildly activated rosin flux.

Note: The mounting conditions described above are offered for guidance only. In all cases temperatures and durations should be minimised whenever possible.

5. BONDING PROCEDURES

Optimum performance will be obtained by bonding two parallel gold wires between designated circuit pads, and the carrier rails. Excessive bond wire inductance will severely degrade RF performance. Bond wire lengths should therefore not exceed 500μm.

Thermocompression wedge bonding is recommended. Gold wire of diameter ≤20 μm, purity 99.99%. elon 2-4% + 0.5, and tensile strength 3.3g is suitable. During bonding, a stage temperature of 120°C, with a bonding wedge tip temperature of 225°C, should be adequate.

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01-908 9000 (switchboard)
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Telex: 923429

Advance Information

GaAs MMIC 8-12 GHz Mixer
GM 1208 A

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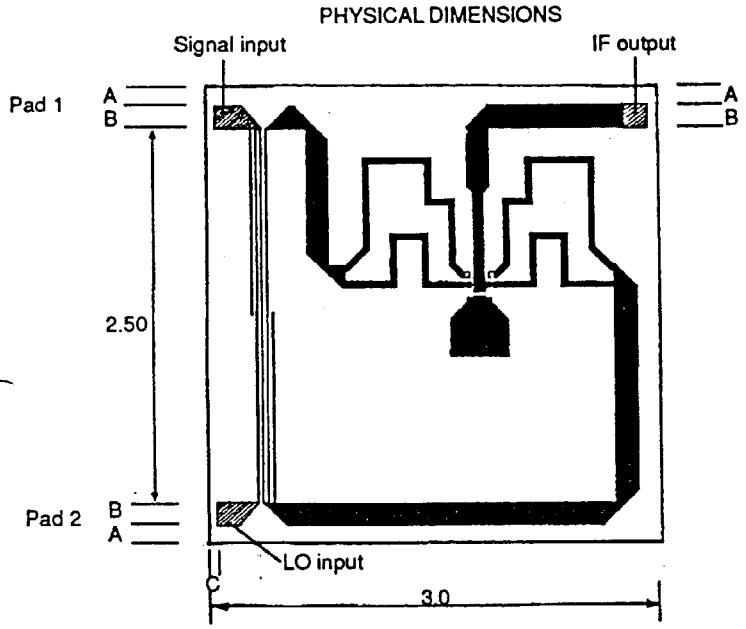
Bond Pad Configuration



Pad 1 Signal Input
Pad 2 Local Oscillator Input
Pad 3 Intermediate Frequency Output

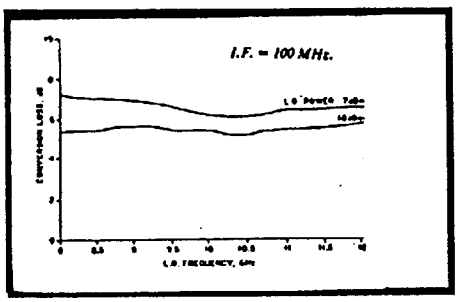
Pad sizes
150µm x 150µm

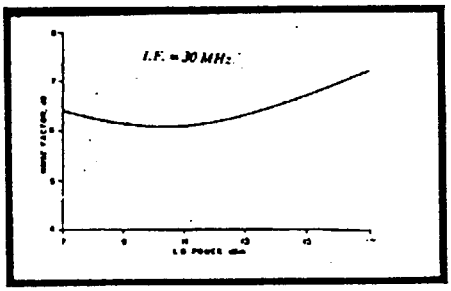
A = 0.1
B = 0.15
C = 0.05

Dimensions in mm
Bonding pads shaded

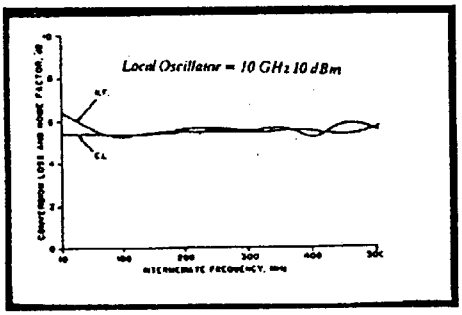
Typical Characteristics at 25° C

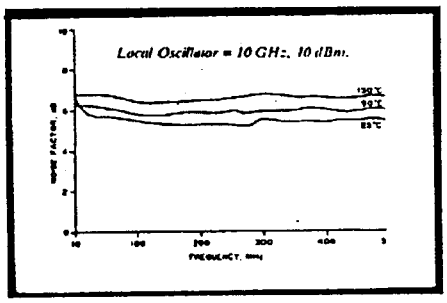
Conversion Loss and Noise Factor





Local Oscillator





Intermediate Frequency

GaAs MMIC 8-12 GHz Mixer
GM 1208 A

Advance Information

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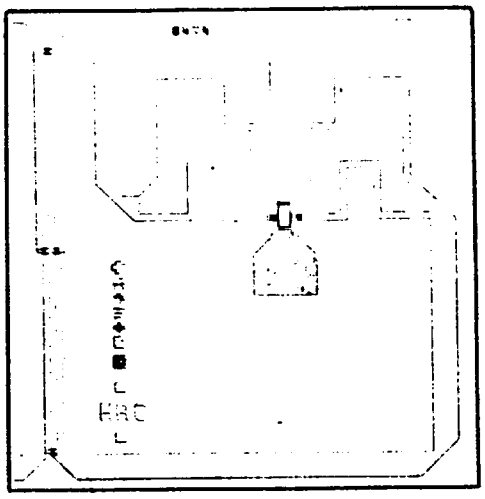
Description

The GM 1208A is a GaAs monolithic microwave integrated circuit single balanced mixer providing low conversion loss over 8-12 GHz.
The circuit employs Schottky barrier diodes to minimise close to carrier noise, enabling operation over a very wide IF range.



Chip size 3mm x 3mm
Chip thickness 200µm

Features

- Schottky diodes
- Extremely wide IF range
- Low conversion loss
- Small size
- Low cost

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Power	P_{IN}	100	mW
Operating Temperature	T_{OP}	-50 to +90	°C
Storage Temperature	T_{STG}	-65 to +160	°C

Electrical Characterisation at 25°C

Parameter	Symbol	Min	Typ	Max	Units	Notes
Signal frequency	f	8	-	12	GHz	1
Intermediate frequency	IF^{sig}	30	-	500	MHz	1
Conversion loss		6		7	dB	1
Isolation, LO - Sig		13	15		dB	1, 2
Return Loss, Sig/ LO ports		8	10		dB	1, 2
IF VSWR				2.5:1		1, 2
Signal Power for 1dB Conversion compression	PdB	5	7		dBm	2, 3
LO drive level	L_O	7	10	13	dBm	2, 3

Notes
1. LO drive = 10dBm, IF = 30MHz
2. f_{sig} = 9-11GHz
3. f_{sig} = 10GHz, IF = 30MHz

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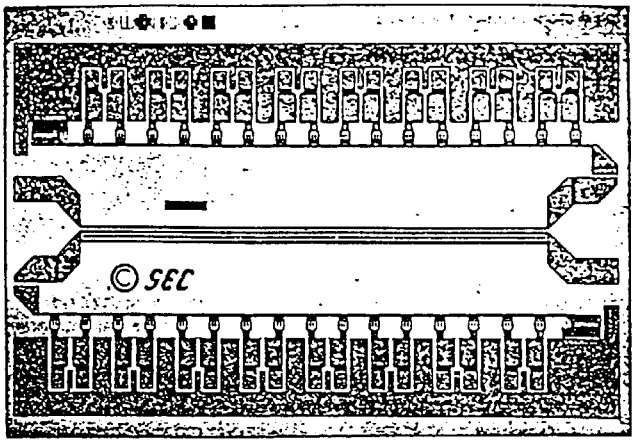
GaAs MMIC 8-12 GHz
4 Bit Phase Shifter

GP 1208 A

Preliminary Information

Description

The GP 1208A is a GaAs monolithic microwave integrated circuit for use as a 4 bit time delay RF phase shifter. The circuit incorporates 32 schottky barrier switching diodes to enable 16 stages at 22.5° increments. The required phase shift is set by forward biasing one of sixteen pairs of diodes.



Chip size 3.8 mm x 2.7 mm
Chip thickness 200 µm

Features

- Time delay
- Low insertion loss (~4dB)
- Small size
- Low cost

Absolute Maximum Rating

Parameter	
On-state current	
Off-state voltage	
Incident RF power	
Storage temperature	~50° to +150°C

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units
On-state current	I_f		50		mA
Off-state voltage	V_r		3		V
Insertion loss	IL		3.5	5	dB
Phase increment at 10 GHz			22.5		Degrees

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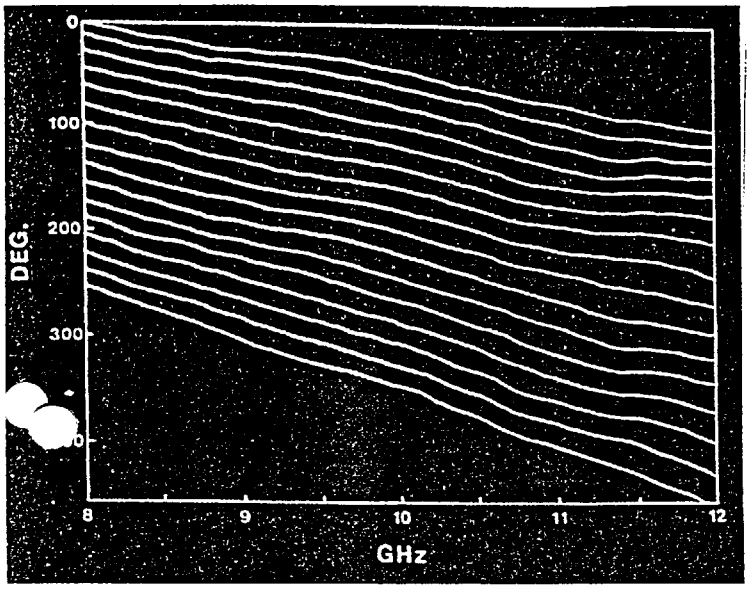
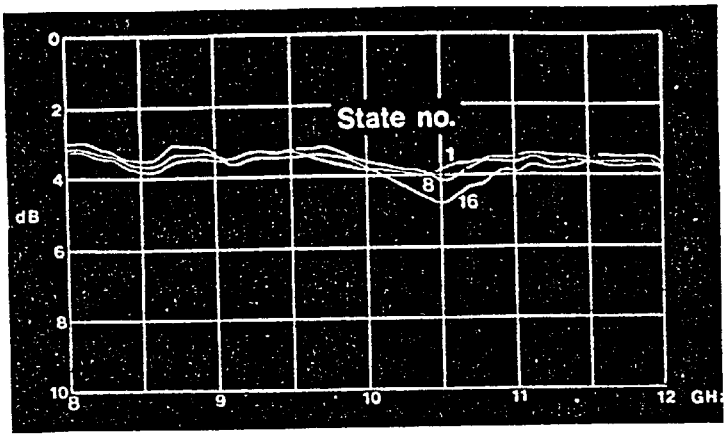
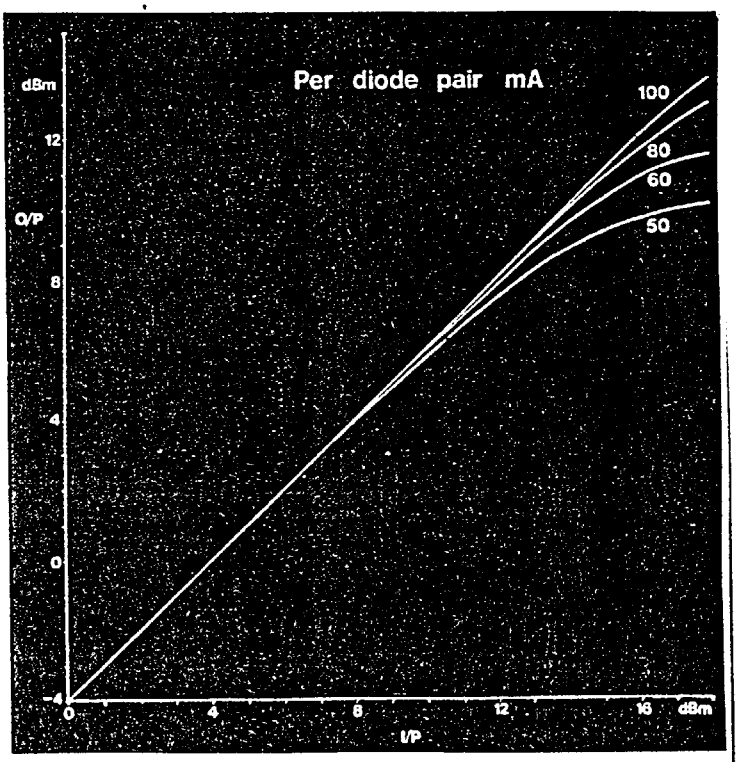
Typical Characteristics



RF Phase Response



RF Insertion Loss



RF Power Handling

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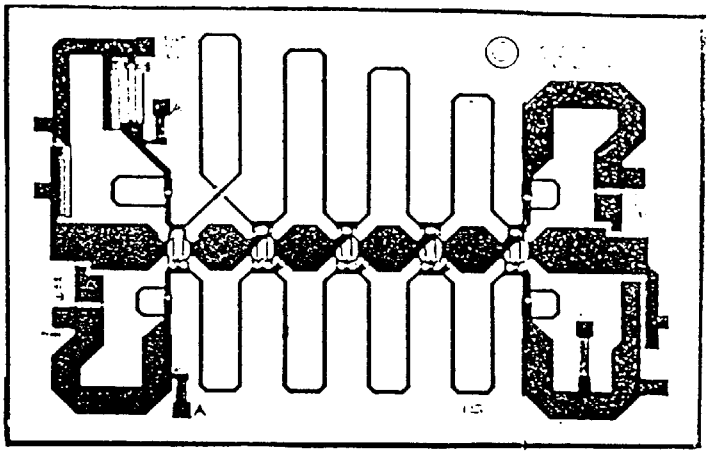
GaAs MMIC 0.5-18GHz Amplifier

GA 1801 A

Preliminary Information

Description

The GA 1801A is a GaAs monolithic microwave integrated circuit for use in broadband low noise amplifiers. The distributed amplifier incorporates five 0.5µm gate length MESFETs.



Chip size 2.5mm x 1.6mm
Chip thickness 150 µm

Features

- Ultra broadband 0.5 to 18 GHz
- Input and output matched to 50 ohm
- Low Noise
- Power output + 15dBm across band
- 0.5 µm directly written gates
- Reliable Ti/Pt/Au gate metallisation
- RF probeable
- Self bias
- DC blocking on RF input and output
- Easily cascadable

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Electrical Characteristics at 25°C

Test conditions V_{DS} = 6V
I_{DS} = I_{DSS}

Parameter	Symbol	Min	Typ	Max	Units	Note
Minimum Frequency	f_{min}		0.3	0.5	GHz	
Maximum Frequency	f_{max}	18			GHz	
Small Signal Gain	G	5.5	7		dB	
Gain Flatness	ΔG		±1.0	±1.5	dB	1
Output power at 1dB compression	P_{1dB}	15			dBm	
Input VSWR				2.0:1		
Output VSWR				2.0:1		
Noise Figure (V_{DS}=3V)			5		dB	
Saturated drain current	I_{DSS}	100	200	300	mA	

Note 1 Frequency range 0.5 to 18 GHz

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Drain supply voltage	V_{DD}	10	V
Drain current	I_D	300	mA
Gate supply voltage	V_{GG}	-10	V
Channel temperature	T_{CH}	150	°C
Storage temperature	T_{STG}	-55 to + 150	°C

Power Supply Requirements

V_{DD} +6V at 150mA

V_{GG} -5V at 5mA

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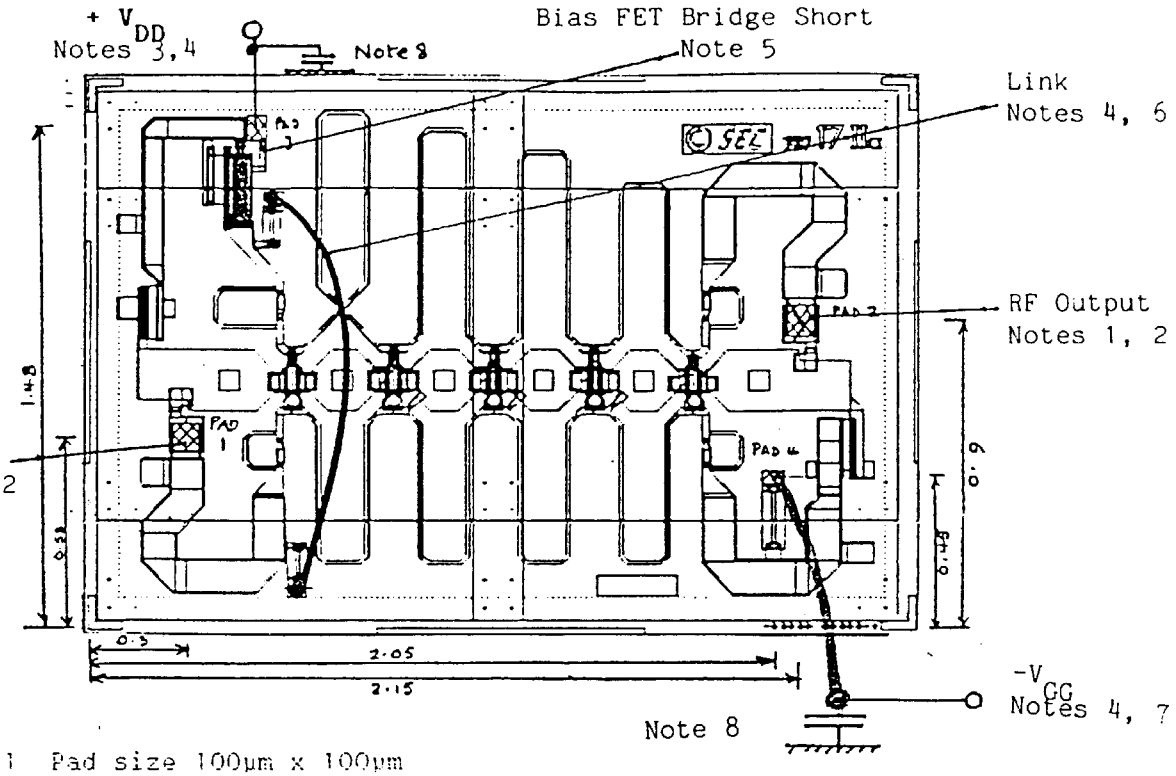
Category E

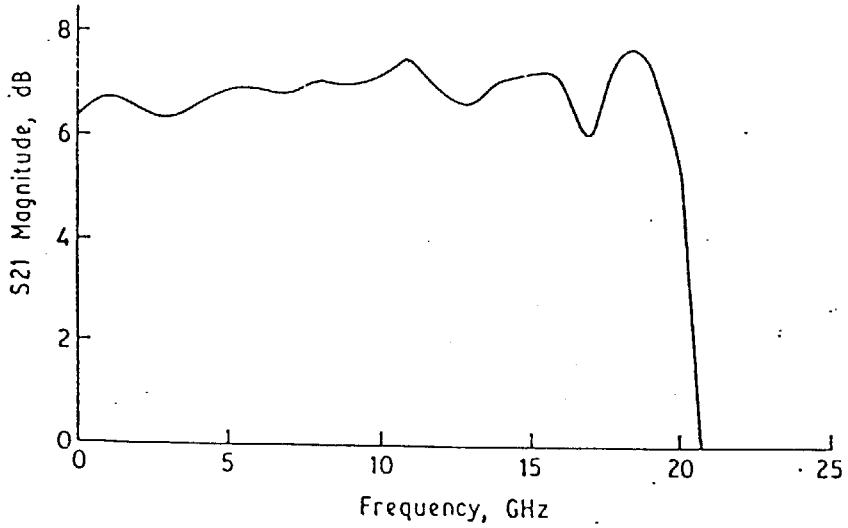
Bond Pad Configuration



NOTES

1. Pad size 100µm x 100µm
2. Recommended bondwire 700µm x 25µm
3. Bias supply +6v
4. Pad size 60µm x 60µm
5. Ensure airbridge shorting bias FET is removed for self-bias operation
6. Connect bondwire 1200µm x 25µm for self-bias operation
7. Bias Supply -6v
8. Bias decoupling capacitor

Typical Characteristics



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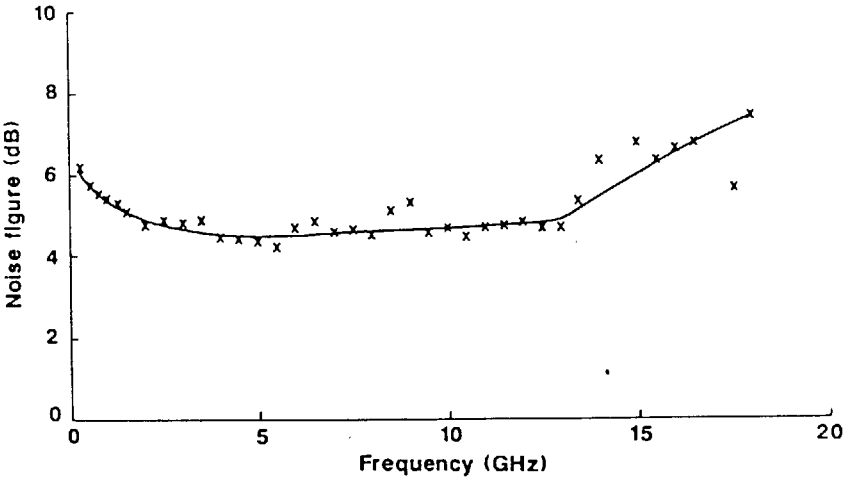
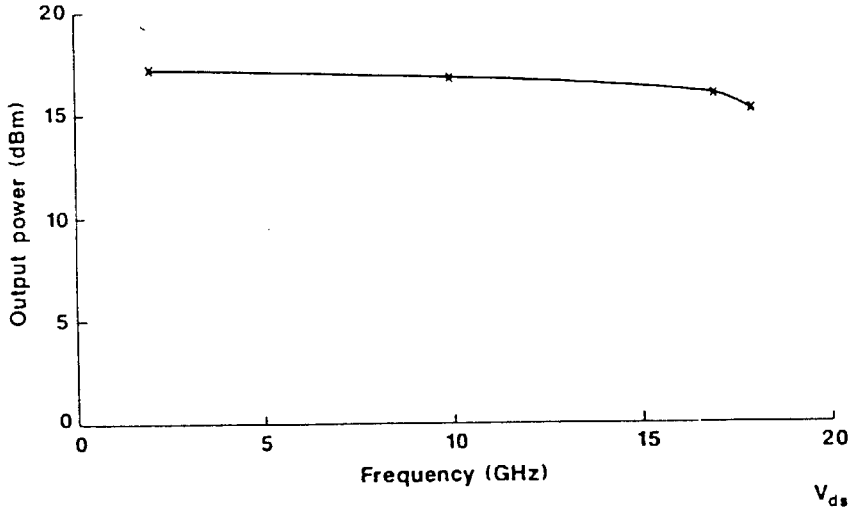
NOISE FIGURE PERFORMANCE



V_{ds} = 3v

0.5 I_{dss}

1dB COMPRESSION POINT



V_{ds} = 5v

0.5 I_{dss}

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Category E

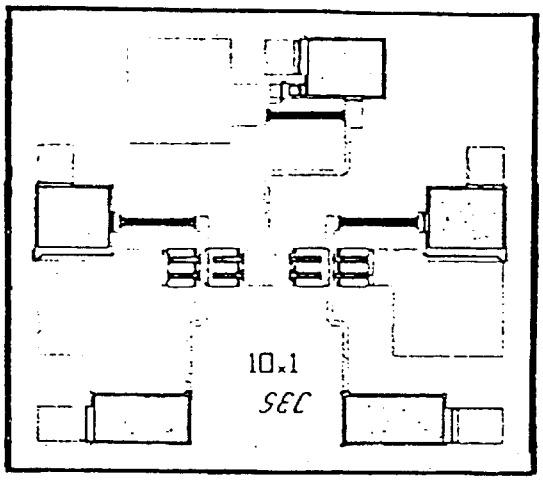
GaAs MMIC 2-18GHz
SPDT PIN Switch

GS 1802 A

Preliminary Information

Description

The GS 1802 A GaAs MMIC SPDT transmission switch is a very fast switching (<10 ns) good power handling device based on PIN diodes. The circuit consists of two pairs of series/shunt PIN diodes to combine ultra-broadband with high isolation and low insertion loss performance. Multi chip assemblies can be used to form multi-pole, multi-throw and extremely high isolation switches.



Chip size 1.5mm x 1.5 mm
Chip thickness 200µm

Features

- Ultra broadband
- Very fast switching
- High power handling
- High isoloation
- Low VSWR
- Small size

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Electrical Characteristics at 25°C

Parameter	Symbol	Frequency	Min	Typ	Max	Units
Insertion Loss	IL	2 GHz		1.2	1.5	
		10 GHz		1.5	1.8	dB
		18 GHz		2.6	3.0	dB
Isolation	Isol	2 GHz				
		10 GHz	35	38		dB
		18 GHz	25	23		dB
Input VSWR		2-18 GHz			2.0:1	
Output VSWR		2-18 GHz			2.0:1	
Power Incident P_{IN} for 1dB compression		2 GHz				
		10 GHz				
		18 GHz				
Switching Time		10% to 90%			10	ns
Control Voltage V_C						
Power (10-20 mA)			-12		12	V
Low DC (5mA)			- 5		5	

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Incident	P_{IN}		W
Control Voltage	V_C		V
Operating Temperature	T_{PO}	-50 to + 90	°C
Storage Temperature	T_{STG}	-65 to +150	°C

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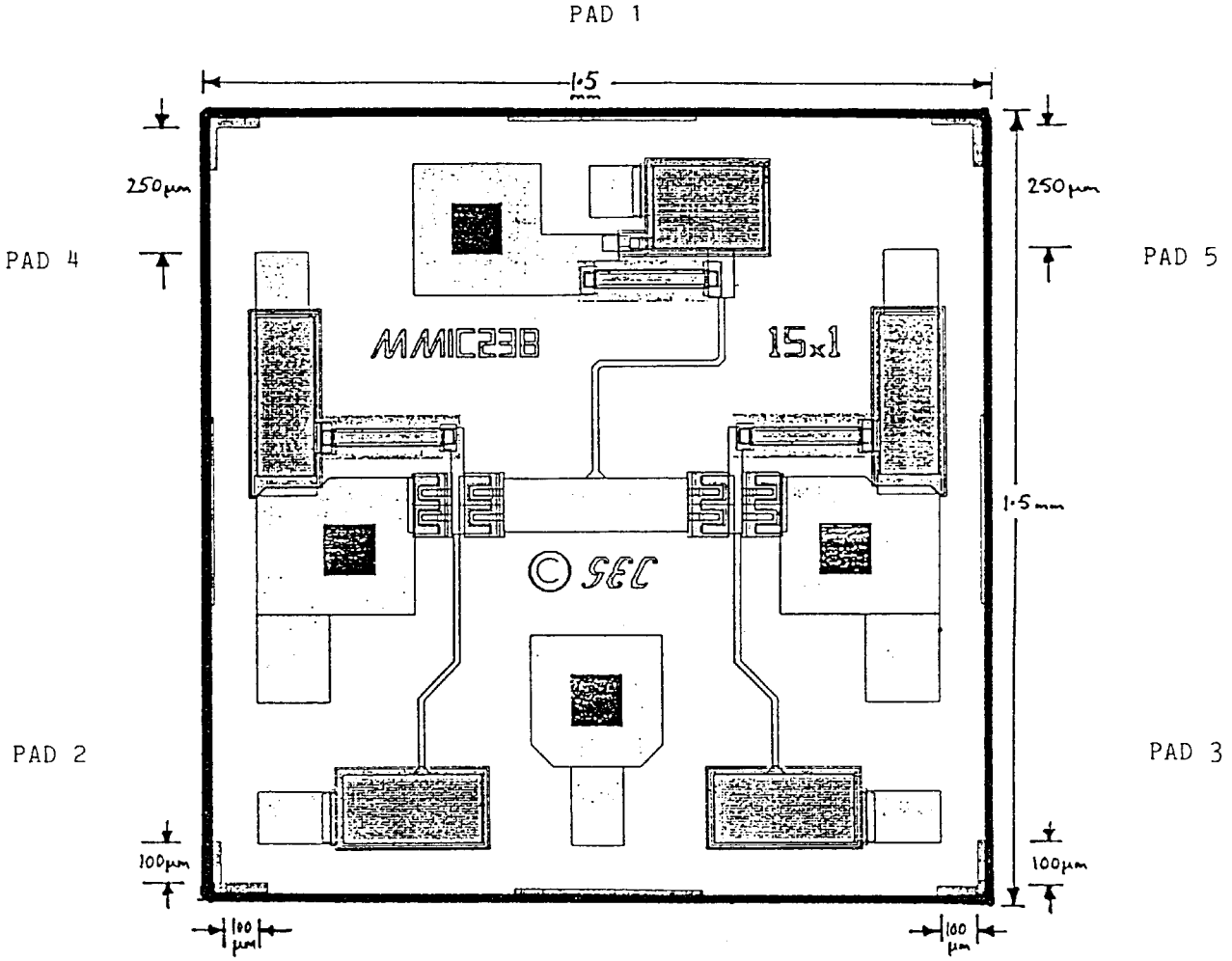
Bond Pad Configuration



PAD 1 - RF input port 1
PAD 2 - RF output port 2
PAD 3 - RF output port 3
PAD 4 - Control Voltage ports 1 & 2
PAD 5 - Control Voltage ports 1 & 3

Bond pad areas 100µm x 100 µm

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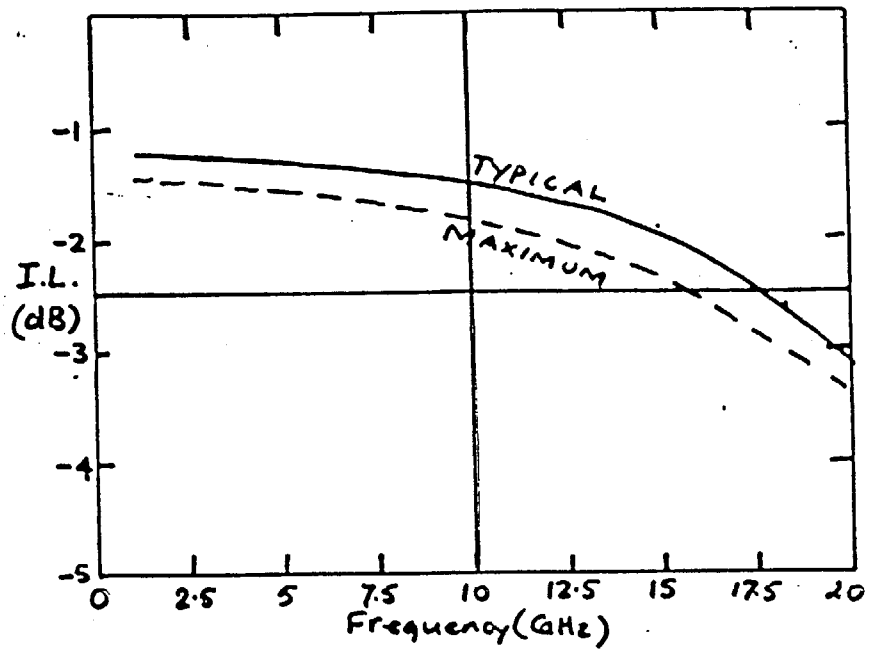
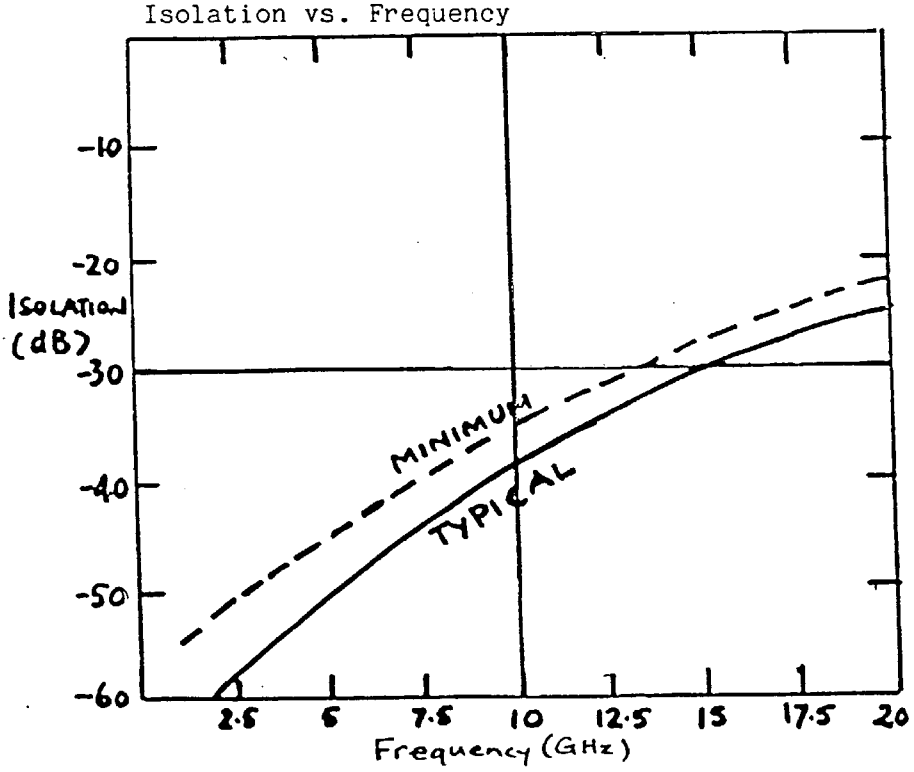
Typical Characteristics at 25°C

Insertion Loss vs. Frequency



Isolation vs. Frequency



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Category B

GaAs MMIC 94 GHz

BALANCED MIXER

GM 9888A

Preliminary Information

Description

The GM 9888A is a GaAs monolithic microwave circuit single balanced mixer for operation at 94 GHz.

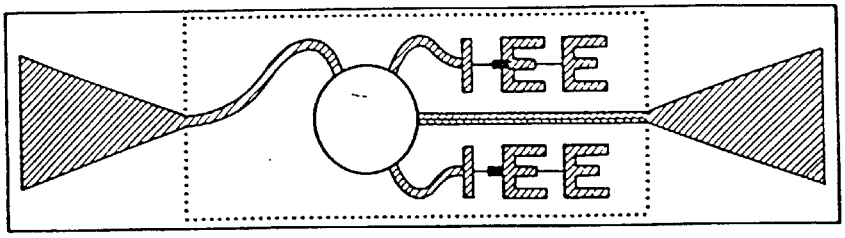
The circuit employs Schottky barrier diodes of air-bridge construction, a 3dB 180° rat-race coupler and r.f. matching elements. Signal and local oscillator access is provided by two on-chip E-plane probes (half 'bow-tie' antennas for direct coupling into waveguides).

A chip variant, i.e. one without probes, permits integration with conventional millimetric Z-cut quartz microstrip MICs.

Features

- Schottky diodes
- Low conversion loss
- Small size
- E-Plane or microstrip coupling
- Low cost

GaAs MMIC 94 GHz MIXER



CHIP LAYOUT 4mm x 1mm

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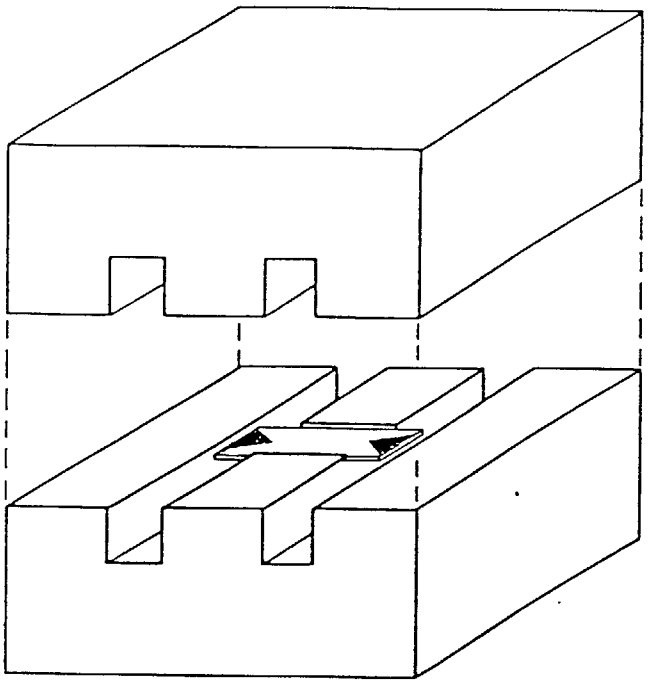
Preliminary Information

GaAs MMIC 94 GHz
BALANCED MIXER
GM 9888A



MOUNTING ARRANGEMENT

ELECTRICAL CHARACTERISTICS AT 25°C

Operating frequency	88-98 GHz
Intermediate frequency	10 MHz-1.0 GHz
Conversion loss	7.5-8.5dB (inc.WG mount losses)
Isolation, LO-Sig	$\geq$20dB
Return loss, Sig/LO ports	$\geq$14dB
LO drive level	5-10dBm

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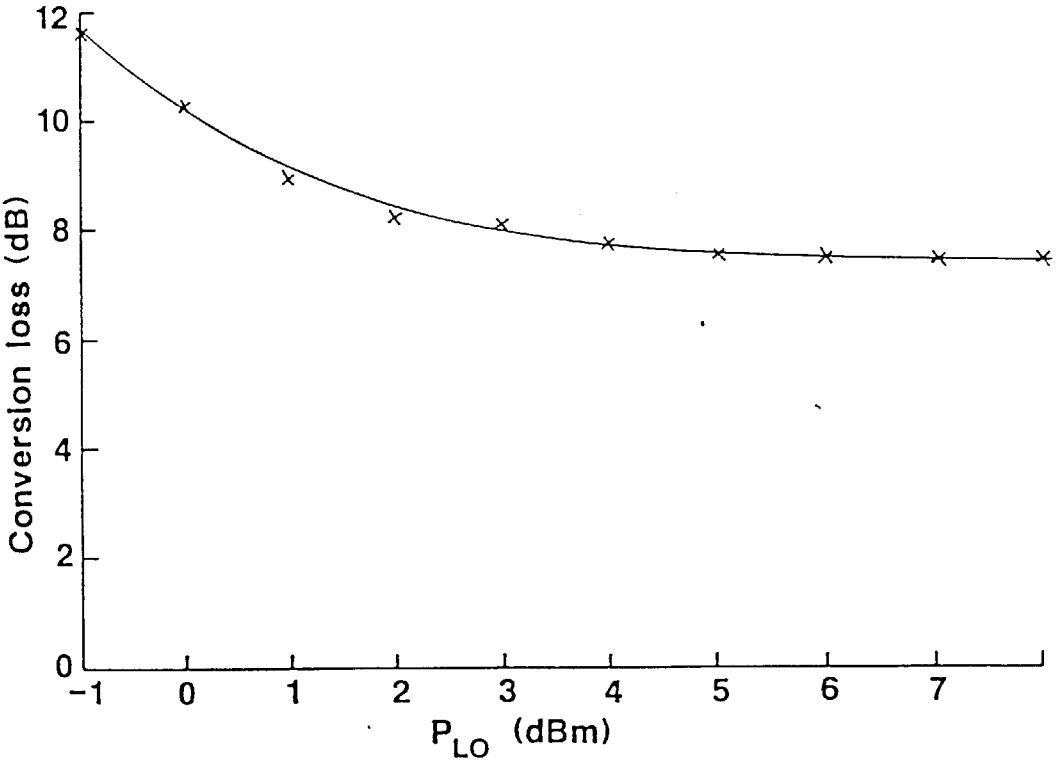
Preliminary Information

GaAs MMIC – 94 GHz MIXER
CONVERSION LOSS vs. P_{LO}



Sample CT1020

F_S = 94 GHz

F_{IF} = 500 MHz

bias = 2.77 mA

(Not corrected for WG mount loss)

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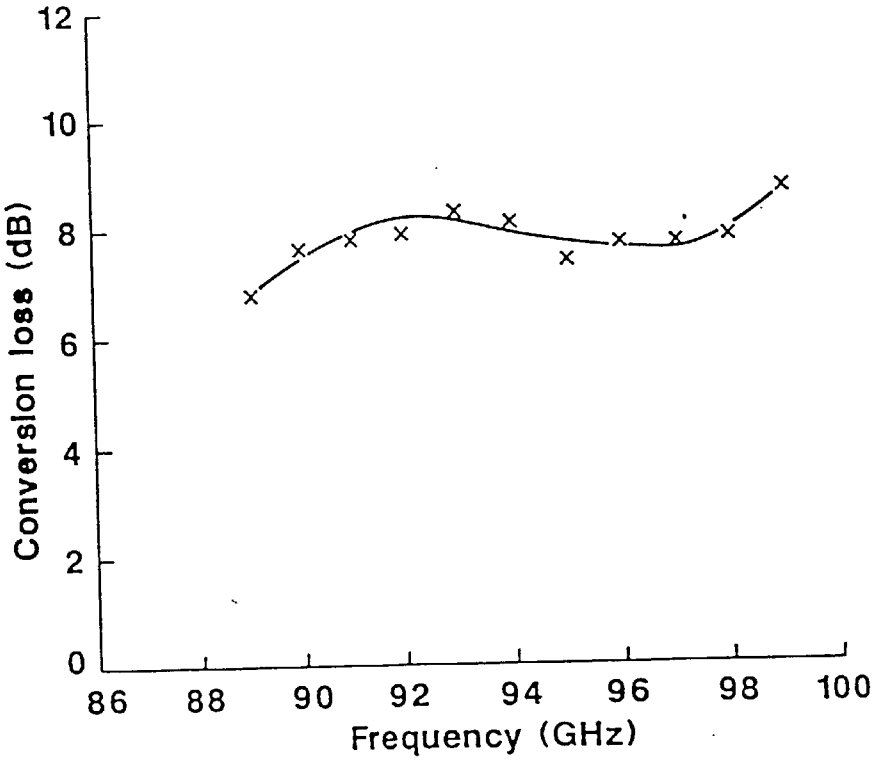
GaAs MMIC 94 GHz MIXER
CONVERSION LOSS vs. FREQUENCY



Sample CT1020

F_{IF} = 500 MHz

P_{LO} = +5dBm

bias ~ 3mA

Not corrected for WG mount losses

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